Full Chip Modelling of ICs under CDM Stress

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9 June, 2005

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de assistent-promotor prof.dr.ir. A.J. Mouthaan

Knowledge of a person not set forth before others is like a flower without fragrance - (free translation from Thirukurral)

To my Parents

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Summary

From the day of the invention of the first transistors until today, the size of the transistors used in the electronic integrated circuits (ICs) has been reduced drastically. With reducing device dimensions, the capability to withstand high voltages across the circuits has also been decreasing. When an IC is subjected to Electrostatic Discharge (ESD), a large current flows from the static charge source to the grounded pin through the circuit. To protect the circuits from being damaged by ESD, large protection devices capable of handling large currents are built into the circuit to provide low impedance paths for the discharge current. During packaging, marking or shifting, ICs can build up static charge due to rubbing of surfaces. When such charged ICs touch a grounded surface, Charged Device Model (CDM) type of ESD is said to occur. The increased usage of automated handlers increases the probability of ICs being subjected to CDM stress, while the scaling down of device dimensions cause the ICs to be vulnerable to CDM damage.

In this thesis, CDM ESD stress on the Integrated Circuits (IC) and the various factors which affect the robustness of an IC design against CDM stress is investigated. One of the main reasons for CDM failure are the voltage gradients set across the circuit during CDM stress. The IC being also the source, its discharge current path is not constrained near the input and output pads as in other kinds of ESD stress. Instead it can be anywhere through the internal circuitry into the ground. The major hinderance in developing a CDM robust protection design is the lack of knowledge on the CDM current and its discharge path through the circuit. CDM withstand level, is package dependent and it is impossible to characterize a circuit design to be CDM robust independent of its package type.

In **chapter two**, the CDM current source is identified and an equivalent circuit model for an IC under CDM stress is proposed.

Protection devices are key elements of any ESD protection. The behavior of some of the commonly used protection devices under fast transient large current CDM stress is studied in **chapter three**.

The input and output buffers form an interface between the outside world and inside core circuit. Hence these circuits at this interface are one of the most vulnerable locations to CDM failure. The CDM guidelines available in the literature recommend the use of large resistors between the protection device and the circuit to be protected. Placement of additional protection devices closer to the device to be protected is also recommended. In **chapter four**, the individual influence of each of these design variations and their effect on the current and voltage transients across the input and out buffers is studied.

The package type plays a significant role in the CDM failure level of a device. As a result, CDM measurements on the same circuit design has to be repeated each time the package type is changed. This consumes a large amount of time and money. In **chapter five**, a suitable method for extrapolating the CDM withstand level of a circuit in one package to other packages. The proposed method is also experimentally verified. This method does require extensive and accurate measurements of the package parasitics.

Among the various CDM current sources, the capacitance formed by the metal plate on which the IC chip is mounted, with the ground surface is the largest. The discharge current path of this capacitor is through the substrate and the circuits into the grounded pin. This discharge causes voltage drop across the substrate and circuit elements ($e.g$ gates). If the voltage drop increases beyond a certain threshold (gate-oxide breakdown voltage), CDM failure is said to occur. The probability of CDM damage from such voltage drops cannot be determined from the existing full-chip CDM circuit model. In **chapter six**, a suitable method of including this capacitance and its discharge current path through the substrate and the circuit during CDM stress is presented.

The application of the proposed method in chapter five, on three different circuit designs (input protection, tie-off cell and level-shifter) is presented in **chapter seven** and **chapter eight**. Chapter seven focusses on pad based protection design and chapter eight on rail based protection design.

Samenvatting

Vanaf de uitvinding van de transistor tot vandaag de dag zijn de afmetingen van transistoren in geïntegreerde schakelingen (IC) drastisch gereduceerd. Hand in hand daarmee is ook het stroomvoerende vermogen van het circuit afgenomen. Wanneer een IC wordt blootgesteld aan één ontlading van statische elektriciteit (ESD) dan gaat er een grote stroom door het circuit lopen van de statische ladingsbron naar een van de geaarde pootjes van het IC. Om het circuit te beschermen tegen de schade die veroorzaakt kan worden door een dergelijke ontlading worden er beschermingselementen ingebouwd. Deze elementen zijn in staat om grote stomen te voeren en vormen een pad van lage impedantie voor de ontlaadstroom.

Tijdens verschillende fases in het fabricage-proces, zoals tijdens behuizen en tijdens markeerstappen, kunnen IC's door wrijving worden opgeladen. Indien een opgeladen IC daarna in aanraking komt met een geaard oppervlak volgt een elektrostatische ontlading van het type "Charged Device Model (CDM)". Door de toegenomen automatisering van transport van halfgeleider-halffabrikaten en ingehuisde IC's is de kans op CDM-stress verhoogd. Daarnaast verhoogt miniaturisatie van het IC kwetsbaarheid voor CDM-schade.

Dit proefschrift onderzoekt de effecten van CDM-ESD-stress op geïntegreerde circuits (IC) en de diverse factoren die een rol spelen in de robustheid van een IC-ontwerp om een CDM-stress te weerstaan. Een van de belangrijkste oorzaken waardoor IC's als gevolg van CDM-stress falen is de gradiënt in de potentiaal over het circuit gedurende de CDM-stress. Omdat het IC zelf de ladingsbron is, wordt het ontladingspad niet beperkt tot de invoer- en uitvoer-aansluitingen, maar kan de stroom overal in het interne circuit naar de aarde vloeien. Het voornaamste obstakel bij de ontwikkeling van een CDM-robuust

beschermingsontwerp is het gebrek aan kennis over de CDM-stroombron en het ontladingspad door het circuit. Het CDM-overlevingsniveau is erg afhankelijk van het soort behuizing dat voor een IC gebruikt wordt en daarom is het onmogelijk om een circuitontwerp te karakteriseren op CDM-robuustheid zonder het type behuizing mee te nemen in de overwegingen.

In **hoofdstuk twee** wordt de bron van de CDM-stroom geïdentificeerd en een equivalent-circuit-model voorgesteld die een IC gedurende een CDM-stress beschrijft.

Beschermingselementen zijn de essentiële onderdelen van iedere ESD-bescherming. **Hoofdstuk drie** onderzoekt het gedrag van de traditioneel gebruikte ESD-beschermingselementen bij de zeer snelle stroomtransiënten die bij CDM-optreden. De invoer- en uitvoer- buffers vormen een verbinding tussen de buitenwereld en het hart van het circuit en zijn daarom de meest voorkomende plaatsen voor een CDM-faallocatie. De in de literatuur beschikbare richtlijnen om ESD bescherming te maken beveelt het gebruik van grote weerstanden tussen het beschermingscircuit en het functionele circuit aan. Daarnaast wordt het gebruik van extra beschermingselementen dichterbij het te beschermen circuit aanbevolen. In **hoofdstuk vier** wordt de invloed van elk van deze ontwerpvariaties en hun gecombineerde effect op de stroom- en spanning-transiënten over de invoer- en uitvoer- buffers bestudeerd.

Het type behuizing speelt een belangrijke rol in de hoogte van het CDM-faalniveau van een element. Als gevolg hiervan dienen CDM-metingen aan hetzelfde circuit herhaald te worden voor elk gebruikte behuizingtype, wat een aanzienlijke hoeveelheid tijd en geld kost. In **hoofdstuk vijf** wordt een methode voorgesteld en geverifieerd om het CDM-overlevingsniveau van een beschermingselement in een bepaald soort behuizing te extrapoleren naar een ander type behuizing. Deze methode vereist een uitgebreide en nauwkeurige karakterisatie van de parasitaire capaciteit en inductie van de behuizing.

Van de diverse oorzaken die kunnen dienen als CDM-stroombron is de capaciteit van de metaalplaat naar geaarde testplaat waarop het circuit gemonteerd is de grootste. De ontladingstroom van deze capaciteit loopt door het substraat via elk mogelijk pad van lage impedantie in het circuitontwerp naar het ontladingspunt. Bij een ontlading van deze substraatcapaciteit kan de spanningsval over het substraat en de circuitelementen, bijvoorbeeld de gate, groot genoeg worden om het falen door CDM te veroorzaken. De kans op CDM-schade veroorzaakt door een dergelijke spanningspiek kan niet worden verkregen met de voorheen beschikbare "volledige-chip-modellen". **Hoofdstuk 6** presenteert een nieuw model waarin de substraatcapaciteit en de ontladingsweg

door het substraat en het circuit gedurende de CDM-ontlading daarvan wordt meegenomen.

De toepassing van de voorgestelde methode om het CDM-gedrag te bestuderen wordt beschreven in **hoofdstuk zeven en acht**.

1 Chapter Introduction

The word "electrostatic-discharge", would mean different things to different people. For a nature lover, ESD would bring to his mind the spectacular lightning in the sky, for a school child the magical way by which hair stands while touching the Van de Graaf generator, and for some others, an unpleasant annoying feeling at the tip of one's finger while touching a metallic door knob on a dry weather day. ESD simply put is the **"Uncontrolled transfer of static charge between two objects at different potentials"**.

Though all objects are electrically neutral, rubbing or sliding of one object against another results in charge separation or static charge accumulation. The amount of static charge accumulated on an object depends on its electron affinity and the rate at which the static charge is dissipated into its environment. The presence of static charge creates an electric field extending into space. When an object at different potential is brought close to it, transfer of static charge occurs through the least impedance path available, until both the objects reach the same potential. ESD can be hazardous and life threatening depending on the amount of voltage built up from charge collection and the relative impedance of the discharge current path. For example, a house on which lighting strikes will be completely burnt down from the enormously large magnitude of discharge current flown into the ground through it. But for an event such as lightning to occur, the amount of static charge collection should be very large so as to create a voltage drop as high as $300,000$V. It would be surprising to learn that we are exposed to ESD almost every day. And the reason why we do not feel it, is simply because the human body cannot sense any electrostatic voltage drop below 3000V. Therefore ESD becomes our topic of discussion only when the voltage drop associated with ESD exceeds our threshold level (> 3000V).

But ESD has become a major concern for semiconductor industries because the minimum threshold level of its products to ESD stress is very low (much below our sensitivity range). As a result more than 30% of the total number of products returned to the industry because of failure is due to ESD stress. [1, 2]. In this chapter, an overview on the different ways in which the ICs gets exposed to ESD stress, the various test methods available for qualification and characterization of IC products for their ESD robustness and the generally available protection circuit designs is presented.

1.1 ESD in Semiconductor Industry

In the race to miniaturize ICs, device dimensions have gone down rapidly and as result the operational voltage levels and the amount of current carrying capabilities of the circuits have gone down. The discharge current accompanying the ESD stress is much larger than the maximum current which can be safely handled by the circuit without being burnt down. As a result the sensitiveness of ICs to ESD damage has increased with modern technology. In other words ICs have become sensitive to even small charge collection. Most of the ICs face ESD stress when they are packaged and shipped before reaching their customer. Hence the IC producers have to quantify the ESD robustness of their products. This is done through a few test methods that mimic real life ESD events on an IC and the stress level above which the IC gets damaged is evaluated. For the ICs to be stamped as ESD robust, they should be able to withstand a certain minimal threshold level set by any of the international organizations like ESDA, [3]. This threshold level varies with different types of ESD stress. Based on the different ways by which an IC can be exposed to ESD events, four types of models are recognized. They are:

- **Human Body Model (HBM):** HBM is a model describing an ESD event, encountered by the IC during human handling. It is a two pin event where the charge from the human body flows to the ground though the IC. A HBM stress of 2000V can result in a discharge current of amplitude 1A with rise time of 10ns and a pulse width of 100ns as shown in figure 1.1. The test method used for HBM qualification of ICs is shown in figure 1.2. A charged human body is modelled by a 100pF capacitor pre-charged to its stress level (body capacitance with ground) and a large series resistance of 1500Ω (body resistance). As per the ESDA standard [4] ICs should withstand a HBM stress level of 2000V to be qualified as HBM robust. The type of failure usually reported on

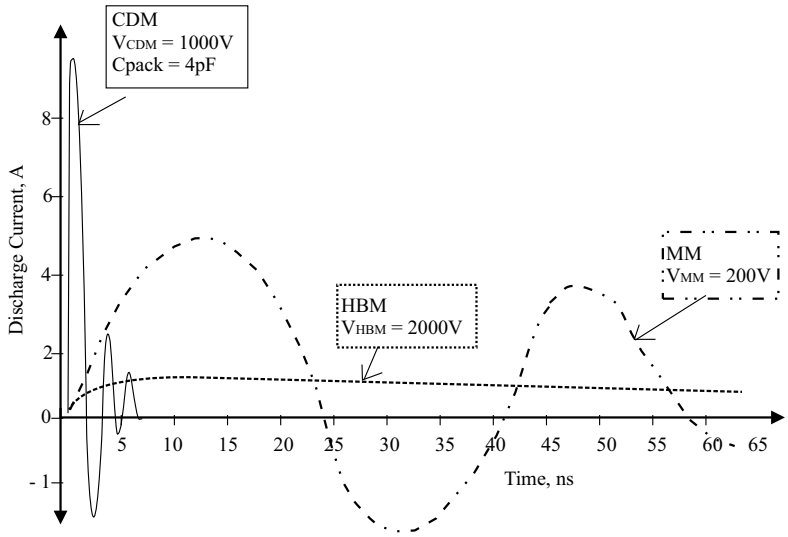


Figure 1.1: Discharge currents during the HBM, MM and CDM ESD .

the IC from HBM stress, is from excess power dissipation at the I/O protection structures [5]. Hence for ICs to be immune to HBM type ESD stress, protection structures should have a low R_{ON}[1]such that the power dissipated in the protection device during the ESD event is lesser than the power needed to melt down the silicon.

- **Machine Model(MM):** MM is a model describing an ESD event encountered when a machine which has static charge touches an IC. A 200V MM stress can generate a discharge current peak of -3.5A with a rise time of 10ns as shown in figure 1.1. The test method used for MM qualification of ICs is shown in figure 1.3. The machines being very good conductors, the impedance offered by it is mainly from its inductance. The capacitance of the machine with the ground is quite large and is modelled by 200pF in the test method. The combination of inductance with large capacitance results in an oscillating discharge current which reaches large amplitudes of current at very low stress levels of even -100V. The ICs are qualified as MM robust, if they could withstand 200V MM stress as per the ESDA standard [6]. The ESD damage on the IC caused from MM ESD stress is similar to that caused from HBM ESD stress, except that the voltage stress level is significantly lower in MM

[1] R_{ON} is the resistance of a device during its conducting (ON) state.

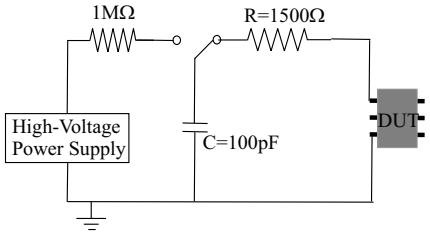


Figure 1.2: HBM test set-up.

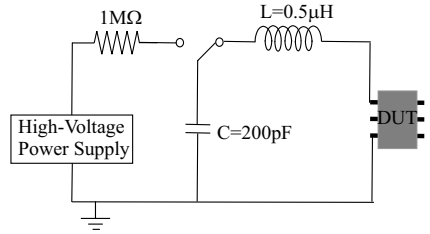


Figure 1.3: MM test set-up.

stress($\approx$ 200V) as compared to HBM($\approx$ 2000V).

- **Charged Device Model (CDM):** When a self charged IC touches a grounded plane, Charged Device Model (CDM) type of ESD event is said to occur. During CDM stress, the static charge stored within the IC flows into the outside ground resulting in a large current flow through the circuit. An equivalent circuit model of an IC under CDM stress is shown in figure 1.4. IC being both the source and part of discharge path, the shape of the discharge current is completely determined by both the IC package parasitics and the circuit design. In general the CDM discharge current has very large current amplitude (few ampere) and a very short rise time (fraction of a ns) and is considered as the most severe kind of ESD stress when compared HBM or MM. A comparison of discharge current waveforms from all three types of ESD events is shown in figure 1.1. As per the ESDA/JEDEC standard ICs should withstand a CDM stress level of 1000V to be qualified as CDM robust [7, 8]. Different test methods used for CDM qualification are explained in detail in chapter 2. A typical CDM failure signature is the presence of gate-oxide failure distributed within the internal circuits as well [9, 10].

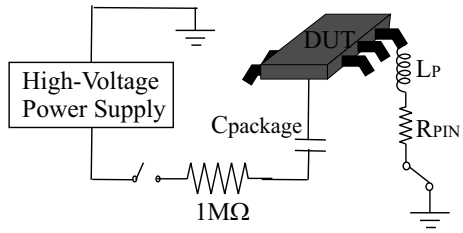


Figure 1.4: CDM test set-up.

- **System level ESD:** The HBM, MM and CDM events model device level ESD event. A system level ESD refers to the ESD event that an IC can encounter when the working system in which it is mounted, is subjected to ESD stress. (It models the ESD encountered by the IC in its working environment). For example, a system can be a Printed Circuit Board (PCB) on which the IC is mounted. System level ESD then refers to the stress encountered by the IC when the PCB is subjected to ESD stress. The test set-up used to study the robustness of system level ESD stress mimics a charged human holding a metallic object and using the metal tip of the object to contact the frame of a piece of equipment [11]. The system level ESD tester circuit consists of a charging capacitor and a discharging resistor. When an ESD event impinges upon the system, the discharge is indirectly coupled to the operating IC as in a CDM stress event. The effect of system level ESD on an IC is equivalent to subjecting an IC to CDM and HBM stress at the same time. System level ESD is gaining increasing attention in last couple of years as it encompasses both CDM and HBM type of ESD events. But this system level ESD is beyond the scope of this thesis and will not be treated in detail.

1.2 ESD Protection Design

ICs can be protected from ESD damage in two ways.

- Prevention: By avoiding exposure of ICs to static charge by use of air ionizers, use of conducting or antistatic bags and packages for transport and use of grounded wrist straps at the work bench while handling the ICs.
- Self-consistent: By making ESD robust circuit design by implementing on-chip protection.

Present industry practice shows that both are necessary to suppress ESD related failures. In this thesis only the second method of ESD protection of ICs is studied. Special protection circuits are built within the IC to avoid the ESD current from flowing into the circuit. Specially designed devices capable of handling large ESD currents and clamping the voltage across the circuit during an ESD event, using a low impedance path are known as Protection Devices (PD). The behavior of these devices will be dealt with in detail in chapter 3. Protection circuits are designed to safely route all the ESD current to the ground through the protection devices, without allowing it to flow

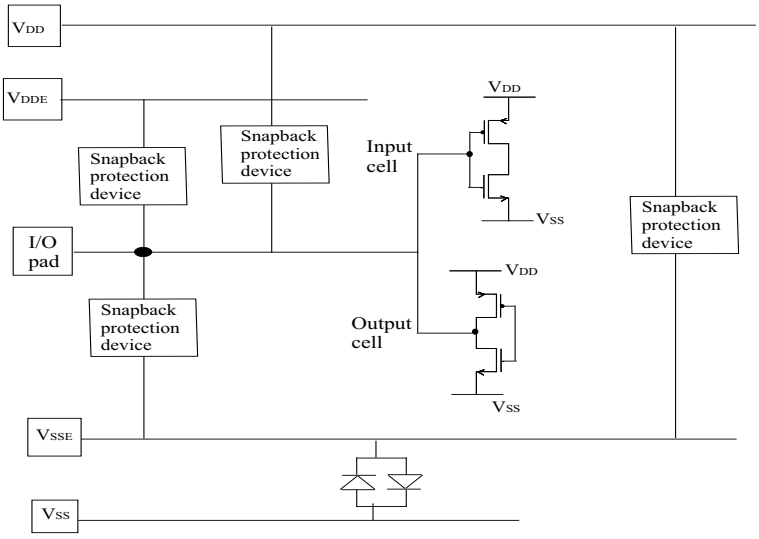


Figure 1.5: Pad based ESD protection design.

through the functional core circuitry. Also care should be taken that the built in protection circuits do not hamper the normal operation of the circuit. Two types of protection designs are generally adopted. They are:

1. **Pad based protection:** A schematic sketch of pad based protection design at the I/O pins is shown in figure 1.5. In this design each I/O pad is clamped to the supply rails by means of one or more protection devices. By this protection design, we make sure that there exists at least one low impedance path through the protection devices, between any two pins during an ESD event. Each V_{DD} pad has a clamping device to the ground line of the circuit but are not connected to other V_{DD} rails. All the protection devices used in this design are typically snapback devices which act more or less as an open under normal operational conditions and as short during ESD stress [12]. The device parameters of the snapback devices changes from one technology node to another. As a result, pad based protection design from one technology node cannot be directly used in another without being optimized.

2. **Rail based protection:** In rail based protection, the supply rails are clamped with each other through a single or series of diodes in its reverse biased mode under normal operational conditions or through an large

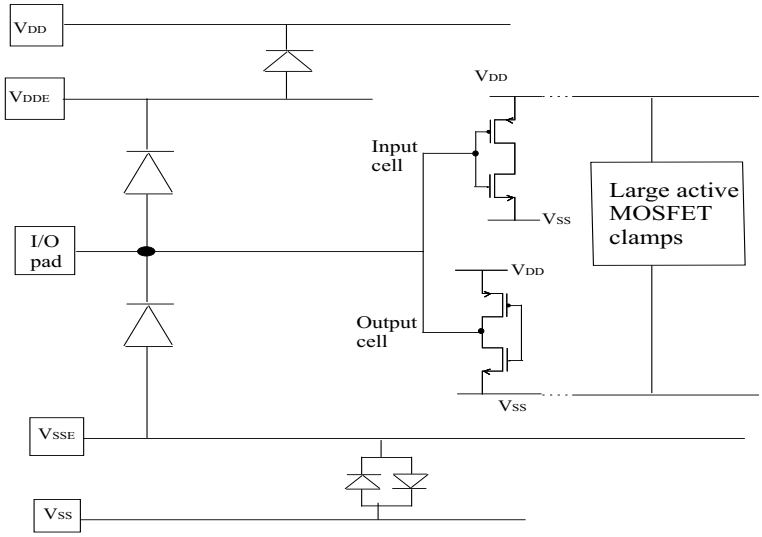


Figure 1.6: Rail based protection design.

active Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFET) or a large Nwell capacitor. Each I/O pad is clamped to the supply rails by a diode in its reverse biased mode under normal operational conditions. In mixed signal circuits, the different V_{DD} rails are also clamped to each other through diodes as shown in the figure 1.6. This avoids any kind of voltage overshoot across the supply rails to exceed beyond a critical voltage level, during its normal operational conditions as well [13]. The device parameters of protection devices used in a rail based protection design mainly diodes, do not change with different technologies. As a result, rail based protection design more preferred as they can be easily transferred from one technology node to another.

1.3 ESD Characterization Methods

The HBM, MM and CDM test methods used for ESD qualification gives the maximum withstand level of the IC but does not help in studying the device behavior during ESD stress. Study of the device behavior during ESD stress is very crucial for optimizing the device layout parameters to achieve maximum ESD robustness. In this section, two types of characterization methods used to

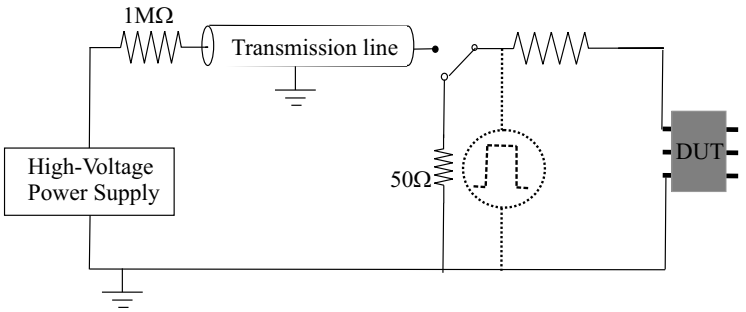


Figure 1.7: TLP test set-up.

study the high current transient behavior of protection structures under HBM like or CDM like ESD stress is explained.

1.3.1 Transmission Line Pulse

Tim Maloney, in the year 1985 [14], suggested the use of Transmission Line Pulse (TLP) in order to characterize the protection circuits during an ESD event. The basic principle TLP consists of charging a 50Ω coaxial cable through a high voltage supply, and then discharging it through a 50Ω resistor as shown in figure 1.7. The resulting waveform is a rectangular voltage pulse, whose pulse width is directly proportional to the length of the transmission line cable and amplitude half of the pre-charged level. Roughly a transmission line of length 1m translates to a voltage pulse of pulse width 10ns. This rectangular voltage pulse is passed through a high resistance R, resulting in a rectangular current pulse. During TLP measurement, this constant current pulse I_{DUT} is driven into the Device Under Test (DUT) and the voltage drop across it V_{DUT} is observed through the oscilloscope. Thus the transient behavior of the device under a given stress level is studied. This process is repeated for higher current amplitudes in specified step size, until the device finally breaks down. The device failure level is studied by performing leakage current measurements under normal operational conditions after each stress level. Thus the high current current and voltage characteristics of the device under high current transients can be extracted from these measurements. A 100ns TLP current source with an impedance of approximately 1 kΩ is used to emulate HBM conditions. It has been shown by several authors [15–19] that the failure threshold level of a circuit from TLP measurements can be correlated to its failure level under HBM and MM stress measurements. Thus it is not surprising that TLP is be-

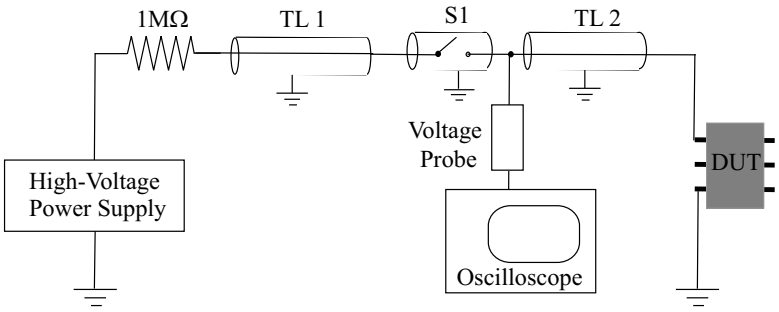


Figure 1.8: vfTLP test set-up.

ing used extensively to both characterize and qualify their IC chips for HBM and MM immunity, by ESD engineers all over the world.

1.3.2 Very fast Transmission Line Pulse

In order to emulate high-current conditions similar to CDM, a large current pulse of rise time closer to CDM rise time is used. Such fast transient (2ns to 3ns) are known as very fast TLP (vfTLP). Realization of a TLP with a very fast current rise time, short pulse duration and high amplitude with the set-up described in section 1.3.1 is very difficult. Hence vf-TLP system was designed as a high-current time domain reflectometer by Horst Gieser [20]. In this system, an incident voltage pulse of short duration defined by the length of TL1 travels from pulse generator to the DUT via TL1 and S1 and is reflected at DUT. The voltage of the incident and the reflected pulses are measured with a voltage probe between S1 and TL2. TL2 is made sufficiently long so as to avoid the overlap of the incident and reflected pulse. In order to obtain V_{DUT} and I_{DUT}, a single waveform record containing incident and reflected pulse is spilt up and the reflected pulse is superimposed on the incident pulse. Attempts are made to characterize device behavior under CDM stress using vf-TLP measurements [21]. But one should not forget that this extrapolation is perfectly agreeable only if the current path is the same in both the cases. CDM stress being a one-pin event, the discharge current path is not exactly the same as in vf-TLP which is basically across any two pins in an IC. Hence the application of vf-TLP stress to study the device behavior under CDM stress is still under debate.

1.4 Scope of this Thesis

With the present modern and future technologies, the threat to ICs from CDM type of ESD stress has increased. This is because increased usage of automated handlers have made the ICs prone to more frequent CDM type of ESD stress. Decreased device dimensions, especially thinning down of gate-oxide thickness has made ICs more vulnerable to CDM damage. Hence it is mandatory to study the various means of protecting the ICs from CDM damage.

The large amplitude and very short rise time of CDM discharge current poses two additional requirements on the protection design. First, large current flow through the small bus line resistance of the metal lines in the circuit can cause significant amount of voltage drop across it adding to the voltage over the protection device. Hence the parasitic bus line resistance has to be taken into consideration as well. Secondly, the protection devices should have turn-on time t_{on}[2] faster than the rise time of the CDM pulse. If not the voltage across the circuit will not be clamped and the large voltage overshoot across the MOSt gates will result in gate-oxide failure [22, 23].

In the case of CDM stress, the IC itself is the source. When any one of the IC pin touches a grounded plane, charge from within the IC, flows into the ground through any low impedance path available in the circuitry. Thus there is no specific discharge path for the CDM current. The protection designs presently used are restricted to the input and output (I/O) cell regions and hence are well suited for any two pin ESD event where the ESD current flows from one pin to another. But with the CDM discharge current being distributed throughout the circuit, there is a need to have a distributed protection design [9, 24]. Also CDM robustness of given circuit design varies from one package to another [25, 26]. There is no clear border between the influence of the package and the circuit design on the CDM performance of a circuit.

vf-TLP measurements can help in studying the high current transient behavior of the individual protection devices. But their replacement to study the behavior of protection device under CDM stress is under question.

CDM measurements gives "pass" or "fail" results and does not provide any insight into the behavior of the circuit under CDM ESD event. Any attempt made to study the current or voltage transients within the internal nodes during CDM stress, results in large intervention on its path through the circuit and thus do not provide any reliable information. On the other hand, circuit sim-

[2] t_{on} is the time taken to change from high impedance OFF state to low impedance ON state.

ulations not only help in evaluating the IC performance but can also be used to access the current and voltage transients at any internal nodes under CDM stress without intervening its circuit behavior. Thus simulations can help in analyzing the CDM behavior and hence in faster optimization of the circuit design.

1.5 Thesis Outline

We know that CDM damage is caused from charge transfer by the IC to a grounded pin. But the answers to basic questions such as "Where is the charge stored? What is the path of charge transfer? What role does the package parasitics play in determining the CDM failure level of an IC? What are the exact IC parameters that influence the CDM performance of an IC?" are not very clear. This thesis attempts to answer the above listed questions. It investigates the various elements of an IC that can influence its CDM behavior, and provides a suitable circuit model of the entire IC under a CDM test set-up. The model is applied to predict the weak locations in the circuit vulnerable to CDM damage. General protection design issues that needs to be considered for designing a CDM robust IC is presented.

In chapter 2, the dynamics of static charge flow through the circuit during a CDM stress in real-life and the closeness of the various test methods used for CDM quantification, to a real-life event is studied. The pros and cons of experimental measurements and simulation studies on circuit behavior under CDM stress are listed. An overview of the circuit models presently used for CDM simulations to study the CDM behavior of an IC and their incompleteness/limitations is presented. The need for a full chip CDM model and various IC properties that needs to be taken into account when developing a full chip circuit model is emphasized. An equivalent circuit that can completely represent an IC under Field induced CDM test set-up is presented in a lumped circuit model.

Protection Devices are one of the most important parts of the protection design. These are the specially designed devices that clamp the voltage across the circuit, by providing a low impedance path during an ESD stress event. In chapter 3, CDM and TLP performance of protection devices with varying layout parameters are studied. The compact circuit model used in our simulations to model the device behavior under CDM stress is explained. The high current transient behavior of the device from simulations is cross checked with TLP and vf-TLP measurements.

I/O protection circuits are one of the most vulnerable locations to gate-oxide failure as the corresponding gate (input) or drain (output) is in direct contact with the discharged pin. In chapter 4, the CDM performance of I/O protection circuits with varying designs is studied. The role of each design parameter on the CDM robustness of the circuit is extracted.

The amount of charge stored within an IC depends on the package type and the failure location depends on the discharge current path through the circuit. Hence there is no clear distinction on the effects of package and circuit design separately on the CDM performance of an IC. As a result, even if the circuit design is the same, CDM measurements have to be repeated each time the package type is changed. In chapter 5, the role of package parasitics and a suitable method for the CDM threshold level of a circuit design in one package to be extrapolated to other packages is investigated. The proposed method is applied to identical test structures in different packages and its correctness verified.

The main source of CDM current is from the capacitance formed by the die attachment plate on which the IC chip is mounted. The discharge path of this capacitor into the grounded pin is through the circuit elements present on the substrate. Thus substrate resistance plays a very crucial role on the CDM performance of the IC. In chapter 6, a suitable method of modelling the substrate capacitance and its discharge path through the various devices in the circuit design during CDM ESD is presented. The effect of substrate resistivity variation on the voltage transients seen across the silicon under CDM stress is studied. The limitations on the circuit model are also presented.

The full chip circuit model is applied to study the CDM behavior of two test circuit designs. The first test circuit has pad based protection design and the second has rail based protection. The effect of substrate contact distributions on the voltage transients across the gate-oxide of the MOSt in the circuit designs are studied in chapter 7 and chapter 8.

2 Chapter IC under CDM Stress

The question on where the static charge is stored and how the charge transfer take place during CDM type of ESD event is still unanswered. In this chapter, the dynamics of CDM current in real-life CDM event and in the test methods used to quantify CDM robustness are studied. An equivalent circuit that can be used to simulate the same transients in the circuit as in one of the test methods namely field induced CDM test set-up is developed.

2.1 Introduction

The danger of IC failure from the discharge of static charge on the IC was first reported by Speakman [27]. Soon it was discovered that CDM type of failure was reported to occur more frequently and the need for CDM protection has become an absolute requirement for all IC products. In order to protect a circuit against ESD damage, one should know its discharge current path through the circuit during ESD stress. For CDM ESD protection, this means one should know the static charge source and its path through the circuit, when one of its pins touches a grounded surface. Any test method or simulation employed/used to study the CDM performance of an IC should cause the CDM current to flow in the same path as it occurs in the real-life CDM ESD event.

The basic understanding on how ICs are charged and how the charge transfer causes damage to an IC in a real-life CDM event is reviewed in this chapter. The various test methods used for CDM quantification, and their resemblance to real-life CDM event is studied. The limitations of CDM measurements and advantages of circuit simulation study over actual measurements are analyzed.

The need for full chip CDM model and the various IC elements that it needs to take into account in developing a CDM circuit model is investigated. An overview of the circuit models presently used to study the CDM behavior of an IC is presented and their incompleteness in modelling the CDM behavior is studied. An equivalent circuit that best represents an IC under field induced CDM test set-up is developed.

2.2 CDM in real-life

When two objects of dissimilar materials collide or rub against each other, transfer of electrons from one to another can occur resulting in static charge creation. This process of electrostatic charge creation is known as triboelectric charging. In the production environment, ICs face triboelectric charging in several ways:

- Usage of tape and reel packaging materials
- Usage of adhesive tapes during assembling
- Rubbing or sliding of IC against the surface of a bag or a tube while shipping
- Usage of device marking equipments which put static charges on the packages of the ICs

Thus we see that charge is accumulated on the package material or on the metal leads of the IC during the various stages of IC processing. Static charge on an insulating surface remains on the surface without moving or spreading out, whereas the static charge collected on a conducting surface spreads out to avoid charge imbalance on its surface. In other words, the charge decay time of conductors is shorter than insulating materials. Therefore it is not unappropriate to assume that the static charge responsible for CDM ESD resides on the insulating package material of the IC. No matter where the charge is present, our concern is how this charge affect the CDM performance of an IC. The charge on the IC package is capacitively coupled to the conducting layers of the IC as shown in figure 2.1. From Gauss' law we know that as charge Q approaches a grounded surface its potential with respect to the grounded surface increases. The gradient of the electric field arising from the presence of charge is given by,

$$\nabla . E = Q/\varepsilon \tag{2.1}$$

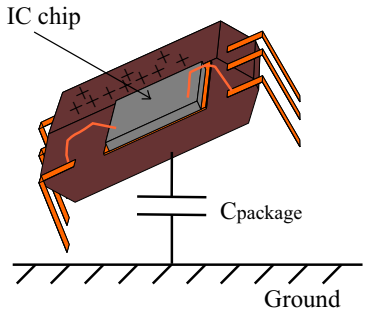


Figure 2.1: CDM in real-life.

where, ε is the permittivity of space. The relative potential of the IC with respect to the ground, just before it touches the grounded plane is given by,

$$V = Q/C \tag{2.2}$$

where,
Q - Charge stored in the IC package,
C - Net capacitive coupling between the conducting layers of the IC and the ground.

When one of the IC pin touches a grounded surface, there is a sudden drop in the potential across the IC, causing charge to flow from the IC to the ground. The amount of charge that flows through the circuit depends on the potential of the IC before it touches the ground and the package capacitance that discharges through the circuit. It is not the presence of static charge itself, but the flow of charge arising from the potential drop developed as a result of charge collection which causes the ESD damage. This is also the reason why some ICs without any static charge but placed in an electrostatic field (or equivalently at different potential) have been reported to have CDM damage.

ESD current arising from CDM stress can be considered as the discharge current of the IC capacitor C_{package}. If we closely examine C_{package}, it is not a single capacitor, but a composite of several capacitors formed by the various conducting layers in the IC with the ground and package as its dielectric. When a particular pin touches a grounded surface, all these capacitors discharge through their connections to the grounded pin. The extent to which each of these capacitors influence the CDM performance of an IC depends on its relative magnitude and its discharge current path to the grounded pin

through the circuit.

2.3 Failure encountered from CDM Stress

Discharge current flow through an IC during CDM stress causes two types of failure.
1) Thermal Failure: One does not expect failure from excess heat dissipation to occur from CDM stress as the stress time is very short [28]. This is also one reason why we cannot make a direct extrapolation of the CDM failure level of a protection device to its failure level under vfTLP stress. Nevertheless thermal failures do occur from CDM stress if there is non-uniform conduction of ESD current through the protection device [1, 29]. This type of failure can be considered as a direct consequence of CDM current flow.

2)Gate-Oxide failure: CDM current flow through the circuit, causes the potential drop seen by the gate-oxides of the MOSt to sometimes exceed its oxide breakdown voltage resulting in gate-oxide damage. This is yet another reason why ICs have become more vulnerable to CDM failure especially with the thinning down of gate-oxide thickness. This indirect effect of the CDM current is most often referred to as "the CDM failure" [30].

2.4 CDM Test Methods

The aim of the test methods are to reproduce the same effect on the IC as it occurs during a real-life CDM event and to help in evaluating the IC's robustness against CDM stress. The amount of charge stored and discharge current path through the circuit should be the same in the test method as in real-life CDM event. Hence the parasitic elements in the test set-up should be kept small such that the amount of charge stored and the discharge current flowing through the circuit is greatly determined only by the IC and not the tester parasitics. A lot of research has been done in developing a test method to duplicate real life CDM events starting from 1980s [31, 32].

2.4.1 Non-Socketed Test Method/CDM

Non-socketed test method was the first test method introduced to simulate CDM stress event. It is also known as the robotic test method. In this test

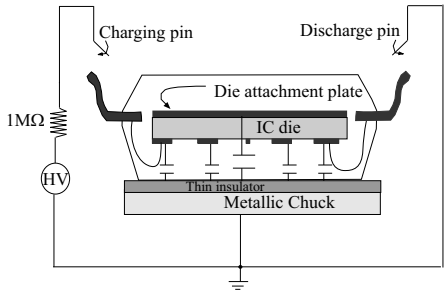


Figure 2.2: Direct contact mode.

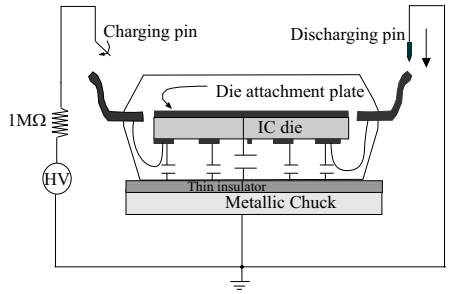


Figure 2.3: Direct non-contact mode.

method, the IC is placed on a metallic plate with its pins facing up (dead bug position). Based on the charging method it can be subdivided into two types, namely,

1. **Direct charge method:** Direct charge method was introduced by Bossard [33] and later developed by others [34]. This method mimics a CDM event which occurs when the IC pin gets charged by triboelectricity. The IC is placed on a grounded plate as shown in figure 2.2 and figure 2.3. The IC is charged either through the pin which provides the best ohmic connection to the substrate or through all the pins simultaneously [7, 8]. The charging process is done slowly so that no damage is encountered during this process and the potential of the entire IC is raised to the electrode's potential. The discharge is initiated by sudden grounding of the pin corresponding to the circuit or device to be tested. The discharge can be done in two modes, the contact mode or the non-contact mode. In contact mode discharge is initiated by an arc within a relay. The relay is metallically connected to the component pin via a socket or probe. And in the non-contact mode, discharge is initiated by an arc between a probe tip and component tip. The main disadvantage is the risk of destroying the IC during the charging up process rather than during discharge.

2. **Field charge method (FCDM):** Field induced charged device model was introduced by Renninger [35]. This is the most commonly used test method for CDM qualification of IC products. This method mimics the CDM event which occurs when the package material of the IC gets charged or when an IC at different potential is subjected to CDM stress. The test set-up for a FCDM test method is shown in figure 2.2. It consists of a metallic plate known as field plate connected to a high voltage supply. By placing the IC on this field plate, the potential of the entire

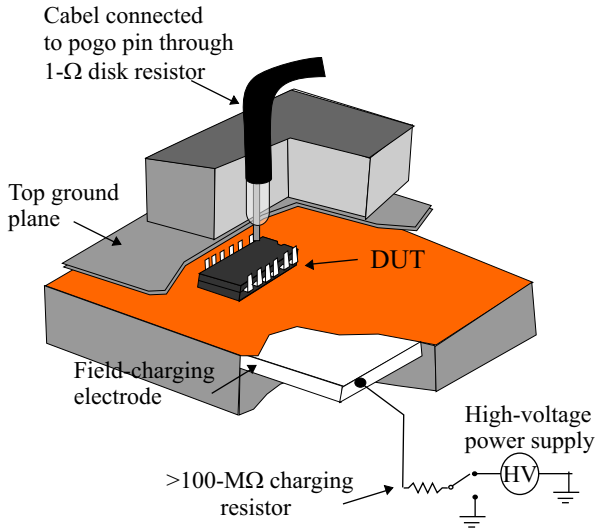


Figure 2.4: FCDM tester set-up.

IC is raised to that of the high voltage supply connected to it. The size of the plate is at least seven times larger in area than the size of the IC to be tested. This is done to ensure that the IC is subjected to uniform electric field and to ensure that there is no potential difference within the IC during the charging up process. The various capacitors within the IC are as shown in figure 2.2. The field-charging plate of the test set-up forms one electrode of the capacitor, the package material and the thin dielectric sheet (used for avoiding charge leakage) represents the dielectric of the capacitors and the various conducting layers in the IC forms the second electrode of the capacitors. Prior to discharge, the field electrode will be at ground and the second electrode (silicon die and the lead frame) will be at the pre-charged potential. Discharge occurs either by contact method or non-contact method where the discharge probe connected to a grounded plane touches or comes close enough to cause ESD of the pin to be CDM stressed. This initiates the discharge of the various IC capacitors through their connections to the grounded pin. Thus the amount of charge stored and the discharge path is greatly determined only by the IC parasitics. The discharge probe is kept small to keep the influence of tester parasitics on the shape of the discharge current minimal. Although the non-socketed test methods mimics a real-life CDM event very well, they have the disadvantage of being very laborious, consuming a large

amount of time. Moreover for ICs with large pin counts and small pitch size (small spacing between adjacent pins), discharge of individual pins cannot be guaranteed by this test method.

2.4.2 Socketed Test Method

The Socketed Test method was introduced to increase the IC manufacturer's CDM testing throughput. This technique has been in progress since 1990 [36]. In this test method the IC is placed in a socket with its pins facing down (live bug position) as shown in figure 2.5. The socket is then charged by a high voltage supply. Discharge is initiated by sudden grounding of the respective pin. By making suitable sockets, individual pins of an IC can be easily addressed even with small pitch size. But the main disadvantage of this test method is that the amount of static charge stored is largely decided by the test set-up parasitics rather than the IC parasitics [25, 37–39]. Hence Socket Test results were found to be independent of the package parasitics whereas in real-life CDM, we observe a strong dependency of CDM robustness on the package type. Because of the large intervention of the parasitics in the test set-up on the CDM test results, the usage of this test method is now restricted to identify the weak products and is not used for product qualification.

2.5 Need for CDM Simulation

The test methods available for CDM quantification help us to know the maximum withstand level of an IC product but does not tell why the circuit design had failed. The post diagnosis of the failure location requires extensive and careful de-processing of the entire circuit design and not the protection device at the I/O region alone. Redesigning of the circuit is done on a trial and error basis which consumes immense amount of time. To design an efficient protection circuit design, it is just not sufficient to know its CDM robustness level alone. Equally important is to know why a protection design is robust or why not. In other words, it is necessary to study the behavior of the circuit under CDM-ESD event. Any attempt made to measure the current or voltage transients within the internal nodes during CDM stress, results in large intervention on the shape of the ESD current and its path through the circuit and thus does not provide any useful information.

On the other hand, simulations help to access the internal circuit nodes without intervening the device or circuit behavior under CDM stress. Study of

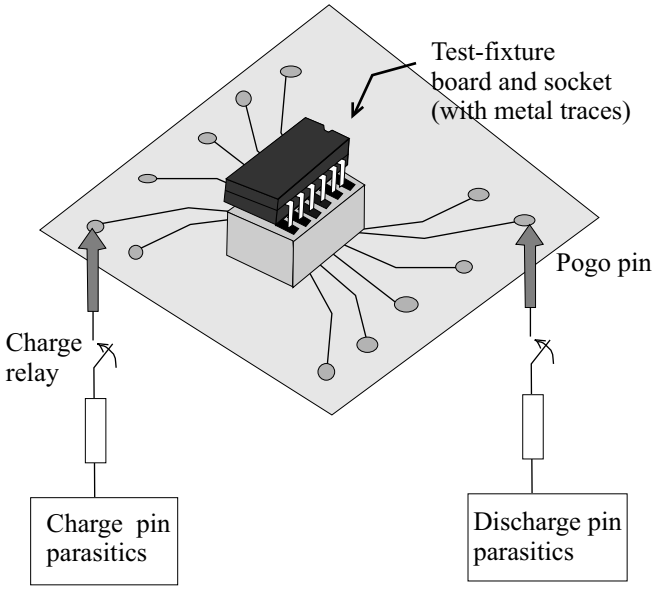


Figure 2.5: FCDM tester set-up.

circuit performance based on simulations gives much faster feedback on the efficiency of the protection circuit design than the time taken in actual production of test samples, testing their CDM performance and evaluating their failure locations. If the CDM circuit model used in the simulations is made as accurate as possible, it can help in designing/redesigning an efficient protection circuit within one or two production cycles and can thus save large amount of time and money.

2.5.1 Requirements for CDM Circuit Model

To protect a circuit from ESD damage, one should know the source of the ESD current and its discharge path through the circuit. For CDM-ESD, the current sources are the various pre-charged capacitors in the IC and the discharge path is the discharge current path of these capacitors to the grounded pin. The circuit model used to evaluate CDM performance of an IC should therefore model the IC capacitors and the circuit elements through which they discharge. For a concise prediction of CDM discharge path in a chip, **"Full-Chip Circuit Model is a MUST for CDM Simulation Studies"**.

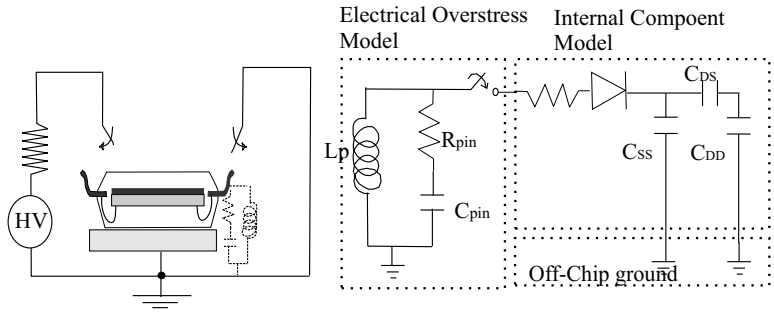


Figure 2.6: Lumped model for chip under direct charge test method by Jaesik Lee.

2.6 CDM circuit simulation - State-of-the-art

Simulations can be classified in two categories, namely device level and circuit level. Device level simulations are focussed on modelling the behavior of devices especially protection devices under high current transients such as CDM-ESD current by using device simulations or compact circuit models [25, 40–42]. Circuit level simulations are used to evaluate the efficiency of I/O protection design under CDM like ESD stress [43, 44]. These simulation studies has helped us to a large extent in understanding and modelling the behavior of protection devices and circuits under fast current transients. But they cannot be applied to evaluate the CDM performance of the entire IC. This is simply because the CDM discharge current is not restricted to the I/O regions, but can be through any low impedance path through the circuit. Moreover these simulation methods do not model the one pin stress condition and the distributed nature of CDM discharge current.

2.6.1 Previous Chip Level Circuit Model

A chip-level simulation methodology for CDM was presented by Jaesik Lee [24]. The model is used to study the transfer of charge from the internal conductors in the circuit design to the grounded pin during a direct charge test method. The entire circuit design is partitioned into subsystems and each subsystem is modelled by an equivalent circuit known as macro model and a full set of such macro models represents the CDM behavior of a whole system. The equivalent circuit of the small subdivisions used to build the entire circuit design is shown in figure 2.6. The CDM current source is modelled by C_{DD} and

C_{SS} which represent the capacitance between V_{DD} and V_{SS} conductive planes and the off-chip system ground, respectively. The capacitance C_{DS}, represents all the capacitance between the on-chip V_{DD} and V_{SS} planes including junction capacitance, oxide capacitance, direct metal-to-metal coupling capacitance, Nwell-to-p-substrate capacitance and decoupling capacitance. When any pin is grounded, rapid charge transfer takes place from C_{SS} and C_{DD} to the grounded contact resulting in a large current flow through the internal components. A large voltage overshoot across C_{DS} during CDM stress simulation indicates the possible location of CDM failure. The circuit model takes into account the distributed nature of the CDM current source and the bus line resistance of the power lines. Also it captures the one pin nature of the CDM stress. The CDM performance of a circuit design is evaluated by studying the voltage drop across the gate and source nodes of MOSts during a CDM stress.

Limitations of the model

The CDM current sources are the several pre-charged capacitors of an IC as explained in section2.2. The contribution of each of these capacitors to the CDM performance of an IC depends on its magnitude and its current path through the circuit. In this respect, the capacitance formed by the die attachment plate, with the system ground or field plate, the substrate capacitance C_{SUB} plays a significant role [45]. This is because of its large magnitude when compared to other capacitors and its discharge path being distributed throughout the entire circuit through the common substrate. Hence a major portion of the discharge current is from the substrate to the discharged pin through any low impedance path available in the circuit design. Grounding of a pin does not only cause voltage drop across the internal nodes of the circuit design but also across the substrate and circuit elements. The voltage drop across the substrate and gate can also result in gate-oxide damage. In the CDM circuit model presented by Lee, the CDM current source is modelled by the power line capacitors C_{DD} and C_{SS} alone. It does not take into account substrate capacitance C_{SUB} and its discharge path through the substrate.

2.6.2 Proposed CDM Model

An IC under FCDM test and its equivalent circuit model is shown in figure 2.7. To make the model less complex, we have neglected the discharge current contribution from capacitance associated with the circuit design, $i.e.$ the capacitance of the metallization lines in the circuit with the field plate is neglected.

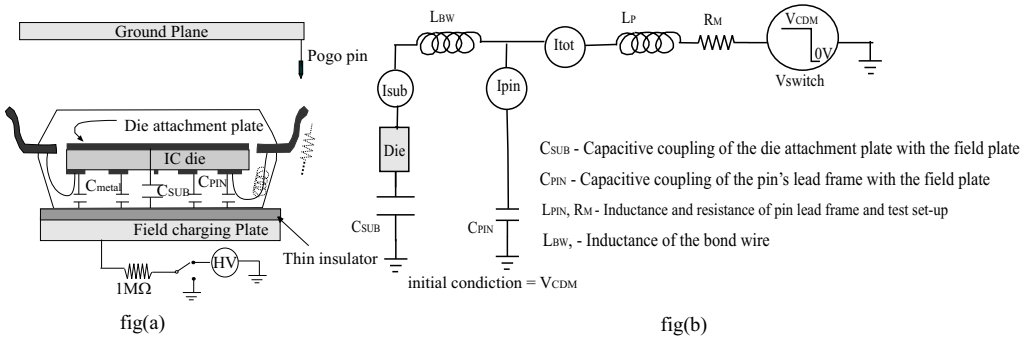


Figure 2.7: Lumped circuit model for a chip under FCDM test method.

This approximation can be justified because of their relatively small contribution to the discharge current when compared to C_{SUB}. The CDM current source is modelled by capacitors C_{SUB} and C_{PIN} which are pre-charged to the CDM stress level say V_{CDM} V. Grounding of the discharged pin is modelled by the sudden drop in the potential of V_{SWITCH} from V_{CDM} to 0V at time $t = 0$ s in the circuit as shown in figure 2.7. In this way, the one pin nature of CDM stress is taken care of. To know the correctness of the simulation model, the discharge current waveform from simulation is compared to the measured discharge current when a complete circuit in a 80 pin QUAD package was subjected to -250V CDM test. The circuit is replaced by a resistor R in the simulation. The package parasitics C_{SUB} and C_{PIN} were measured using a C-V meter at 1MHz frequency at 30mV and L_{P}, the inductance of the pin is taken as the summation of the pin inductance (from RLC measurements of the package) and that of the pogo pin of the tester. The value of resistor R which matches closer to the measured discharge current was chosen to replace the die and circuit. Figure 2.8 shows that the simulated and measured CDM discharge current waveform agrees to a reasonable degree of accuracy. The discrepancies in the simulated and observed results can be attributed partly due to the elementary lumped model of the die used in the simulation and partly to the additional parasitic values from the CDM tester used for measuring. Note that the total discharge current is the sum of the discharge currents from C_{PIN} and C_{SUB}. However, only the current from the latter is of significance as it represents the actual current that flows through the circuit and causes CDM damage in the IC. The equivalent circuit model shown in figure 2.7 is partly incomplete because the silicon die along with the circuit is lumped into one resistor. To be able to use this circuit model to study the CDM performance of a given circuit design,

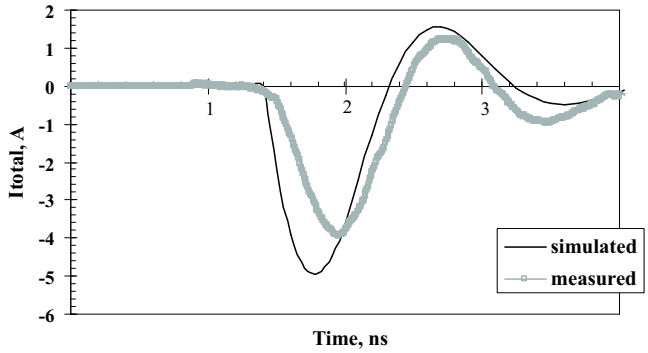


Figure 2.8: Measured and simulated total discharge current of an IC in a QUAD 80 pin package.

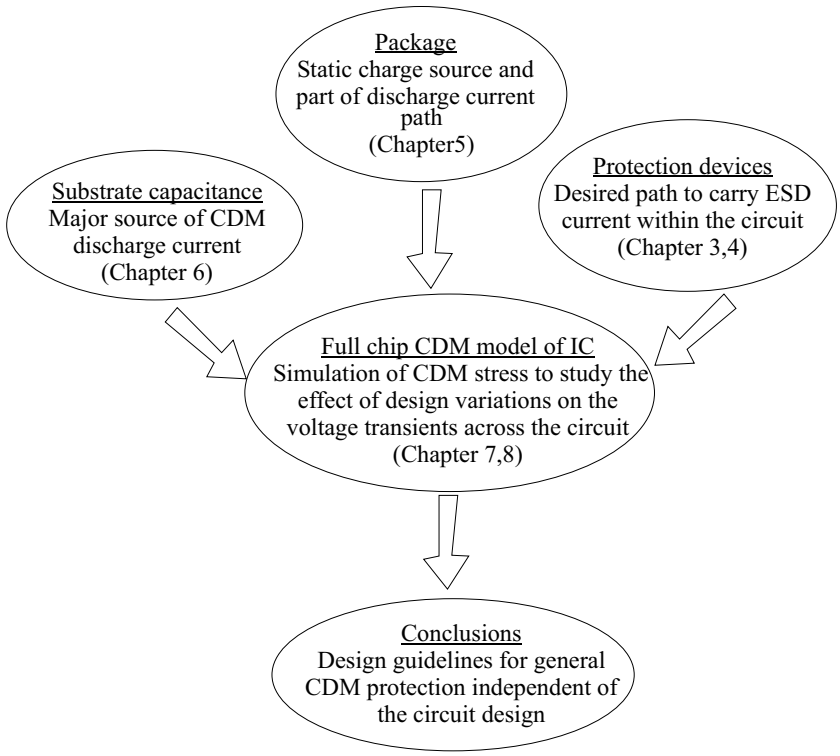


Figure 2.9: Overview on composition and content of this work.

the resistor representing the circuit has to be further expanded to include the distributed nature of the discharge current through the circuit. In other words, the silicon die along with the substrate and the circuit elements and protection devices should be replaced by their equivalent CDM circuit models instead of a lumped resistor. detailed the need for a full chip circuit model to study the CDM performance of an IC, the rest of the chapters are organized as shown in the flow-chart 2.9, to address the various aspects of an IC that needs to be modelled and their role in determining the IC's CDM performance.

2.7 Conclusions

In this chapter, the basic phenomenon of charge transfer during CDM-ESD event is studied. The limitations of experimental measurements in evaluating the CDM performance of an IC and the need for circuit simulations is emphasized. A full chip lumped circuit that models the transfer through and IC during CDM stress event is proposed.

3 Chapter
Protection Devices

The aim of a protection circuit is to route the electrostatic discharge (ESD) current safely into the ground through some special devices in the circuit, capable of handling large currents. The properties of these devices which make them suitable candidates for ESD protection is outlined and the special requirements on these devices for CDM protection is briefed. Influence of layout parameters on the CDM robustness level are studied for few commonly used protection devices like grounded gate MOS transistor (ggMOS) and low voltage triggered SCR transistor (LVTSCR) from experimental measurements. Further, a compact circuit model for MOS which can simulate its high current transient behavior during CDM stress is presented.

3.1 Introduction

To protect the ICs from ESD damage, special protection circuits are built-in into the IC design. The aim of the protection circuit is to route the ESD current safely to the nearest ground, without damaging the circuit. These protection circuits consist of special devices known as protection devices. Ideally speaking protection devices act as an open under normal operational conditions, drawing zero current through it and as short under ESD conditions, drawing all the ESD current through it into the ground. Figure 3.1 shows the ideal *I-V* characteristics of a protection device. ESD currents from CDM stress reach large amplitudes (few ampere) in a very short rise time (fraction of a ns). This fast transient characteristic of CDM discharge current places an additional requirement on the protection device to have a turn-on time shorter than the rise

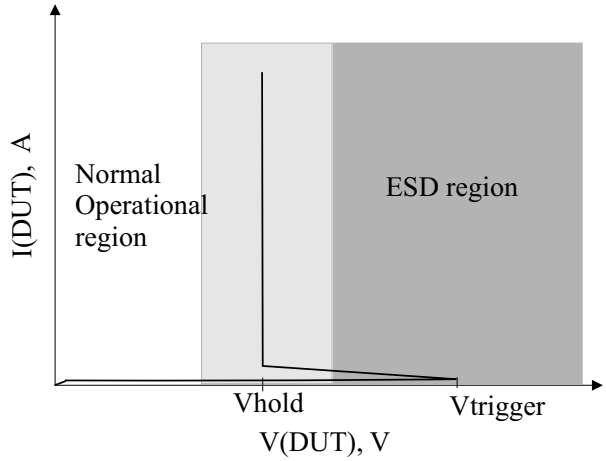


Figure 3.1: *I-V* curve of an ideal protection device.

time of the CDM pulse. In this chapter, the high current transient behavior of some of the most commonly used protection devices and the influence of their layout parameters on its CDM threshold/failure levels is studied. An efficient compact transistor model for MOSt's under CDM stress is developed in the SPECTRE simulator environment and the simulated high current transient behavior compared with TLP and vf-TLP measurements.

3.2 Device physics

Protection devices form the core of a ESD Protection circuit. To design devices that can handle large ESD currents, it is important to study their device behavior under such large current transients. The physics behind the operation of some of the most commonly used protection devices is elaborated in this section.

3.2.1 Diodes

Diodes are the most simple of all devices and are one of the most commonly used protection device. The *I-V* characteristic of a diode and its design layout on a circuit are shown in fig(a) and fig(b) of figure 3.2. One end of the diode is connected to the circuit while the other end is the actual substrate.

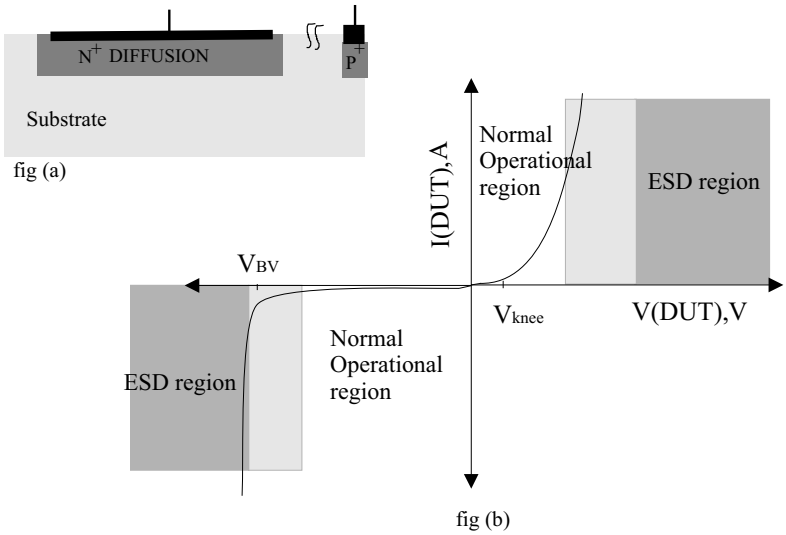


Figure 3.2: fig(a) - layout of the diode and fig(b) - *I-V* characteristic of a diode under different regions of operation.

The substrate connects to the ground line through the substrate contacts. Under CDM like stress, where the current path is mainly from the substrate to the discharged pin, diode can be considered as a one pin device. The series substrate resistance between the diode and the substrate contact will not be in the CDM discharge current path and hence one may expect a better CDM performance of the diodes as compared to diodes subjected to other ESD stress. This can be true only if the substrate at the diode location is well connected to the ground or supply lines which are connected to the I/O pins. In their forward biased mode, they act as high conducting devices providing low impedance. This is the most preferred state for ESD current. In the reverse biased mode, they do not conduct current until the junction reaches its breakdown voltage. Beyond breakdown voltage, it becomes highly conducting. But as the current conduction through the device is from an avalanche breakdown junction, the diode is in a very unstable state and the devices can easily burn down when operated in this region during the entire duration of the ESD stress. Diodes in the protection circuit are built in such a way that during the normal operation of the IC, these devices are in reverse biased state and are in forward biased state in the worst case scenario of ESD stress.

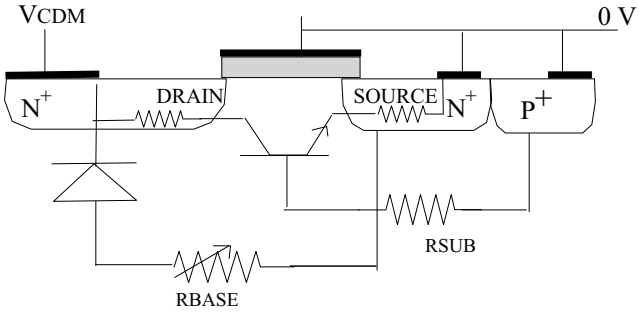


Figure 3.3: Layout of ggNMOSt.

3.2.2 ggMOSt

A MOSt, whose gate node is shorted to its source node is the most commonly used protection device in CMOS technology. Under normal operational conditions this device offers very high impedance and thus acts as an open. Under high current conditions, it is not the MOSt which turns on but the parasitic device present in the MOSt that turns on providing a very low impedance path. This property of the device is utilized for ESD protection. The device physics of a grounded gate n-channel MOS transistor (ggNMOSt) is explained below. The explanation remains the same for grounded gate p-channel MOS transistor ggPMOSt except for the fact that the electrons should be replaced by holes.

ggNMOSt under two pin stress

Two pin device behavior represents the device behavior when the stress is across two pins, namely the drain and source of the device. The layout of a ggNMOSt and the parasitic devices that become active when high current stress is applied across drain and source nodes of the ggNMOSt is shown in figure 3.3. When the drain is subjected to positive ESD stress with respect to source, a parasitic Lateral -Bipolar Junction Transistor (L-BJT) is activated. The operation of the L-BJT under ESD stress can be subdivided into four regions. The current and voltage transients across the device in these four regions are shown in figure 3.4.

1. As the voltage across the device is raised, the drain-bulk junction gets reverse biased and only the junction leakage current flows through substrate resistance R_{SUB}.

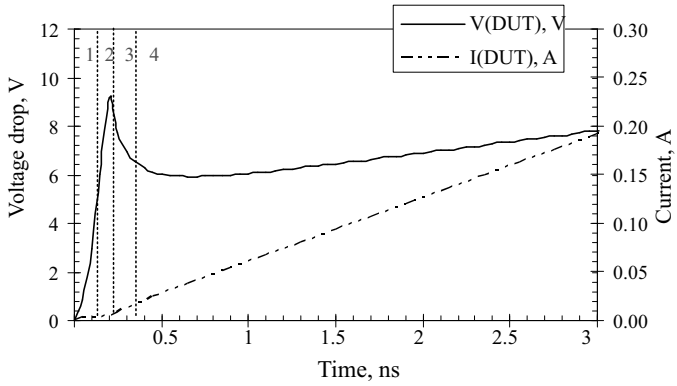


Figure 3.4: Current and Voltage transients across the ggNMOSt (L-BLT) in its different regions operation.

2. When the potential across the drain-bulk junction approaches its junction breakdown potential, the leakage current from the junction flowing through R_{SUB} increases drastically, while the potential across the drain-bulk junction is clamped at its junction breakdown potential until the potential drop across R_{SUB} exceeds the knee voltage ($0.7V$ for Si), and forward biases the source-bulk junction and begins to pump electrons into the bulk and holes into the source. The time taken for the source-bulk junction to get forward biased depends on value of R_{SUB}. The larger the value of R_{SUB}, the lesser is the time taken to forward bias the source-bulk junction.

3. Most of the electrons feedback into the bulk enter the depletion region (space charge) of the drain-bulk junction and undergo avalanche multiplication due to the presence of very high electric field. This avalanche current source supplies enough current for the source-bulk junction to be forward biased and pulls down the potential across the device to a holding voltage V_{H}. The drop in the potential across the device is a function of its drain-bulk junction potential and the fraction of the current feedback into the depletion region of the drain-bulk junction. The higher the multiplication factor, the lower is the holding potential. The time taken for the electrons from forward biased junction to be feedback into the depletion region is the transit time of the device, which depends on the gate-length (channel length) of the MOSt.

4. Further increase in the applied potential, only increases the current flow-

ing through the device and the potential drop across the device is given by,

$$V_{\text{DEV}} = V_{\text{H}} + I_{\text{ESD}}.R_{\text{ON}} \tag{3.1}$$

where,

$$R_{\text{ON}} = R_{\text{drain}} + R_{\text{source}} + R_{\text{base}} \tag{3.2}$$

R_{drain} - resistance between the drain contact and the drain substrate junction,
R_{source} - resistance between the source contact and the source substrate junction,
R_{base} - resistance of the bulk channel/resistance of the base between the two junctions.
The turn-on time t_{on} of a device can be defined as the time taken for the device to change from its "OFF" state to "ON" state. That is the time taken for the device to reduce the voltage drop across it from junction breakdown potential V_{BV} to V_{H}.

$$t_{\text{on}} = t_1 + t_2 \tag{3.3}$$

where,
t_1 - time lag between the on-set of junction breakdown potential and turning on of the source-bulk junction,
t_2 - time taken for electrons to be fedback from the forward biased source-bulk junction to the depletion region at the drain-bulk junction.

Thus the device parameters that determine t_1 and t_2 are R_{SUB} and gate-length of the device.

When the drain is stressed negatively with respect to the source, the parasitic diode formed by the drain-bulk junction gets turned on. This diode is different from drain-bulk junction active in the L-BJT model in the sense that the area involved here is the entire drain-bulk junction below the drain, while it is the sidewall junction in the case of the parasitic L-BJT. Because of the high current injection, conductivity modulation[1] of the R_{BULK} occurs resulting in the lowering of the effective base resistance.

ggNMOSt under two pin stress

The device behavior as explained in section 3.2.2 holds good for a two pin stress event like TLP and HBM stress when the ESD stress is applied across

[1]Conductivity Modulation is said to occur when the number of mobile carriers injected exceeds the doping concentration in the neutral region because of high current injection

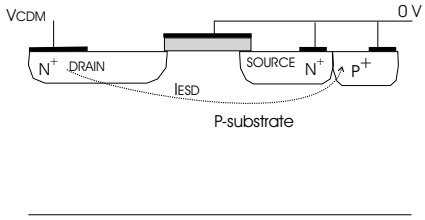


Figure 3.5: two pin ESD.

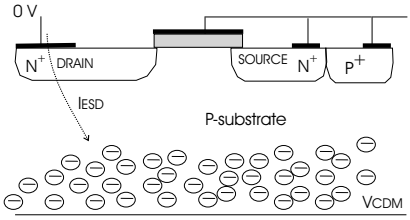


Figure 3.6: one pin ESD.

the drain and source of the protection device. See figure 3.5. But for CDM stress event, the stress is across the drain and the entire p-substrate as shown in figure 3.6. Unlike other ESD events where the source and substrate contacts are fixed at a particular potential, here they are left to float and its potential depends on the potential of the p-substrate below.

Let us consider an IC test structure with individual ggNMOSts with varying layout parameters subjected to negative CDM stress. When a pin of this pre-charged IC, corresponding to the drain of a ggNMOSt is grounded, electrons flow into the ground, setting a potential gradient across the substrate. Substrate closer to the grounded drain will begin to rise in potential, while the other regions still remain closer to the pre-charged potential level. If the substrate contact is unique to that MOSt under test, then the potential of the substrate contact and source will not vary very much from that of the bulk region below the drain. In such cases, the potential drop across R_{SUB} can be much smaller than the knee voltage of the source-bulk junction, needed to turn on the L-BJT. But in reality, the V_{SS} lines shorts all the substrate contacts spread out in the circuit, and is hence effectively coupled to much larger substrate capacitance. This implies that the potential of the substrate contact remains closer to the applied stress level V_{CDM} and hence the explanation for the device behavior under two pin stress event can also be applied to the one pin CDM-ESD stress, provided the substrate contact of the MOSt under test, is strongly coupled to the p-substrate.

These two situations, wherein the source contact is unique to the device and the when the source contacts are common to all devices within the circuit can be represented by a circuit as shown in figure 3.7. The charge source and its discharge path to the grounded pin is modelled as lumped capacitors and resistors. Each circuit element is coupled to the substrate capacitance depending on its area of contact to the substrate capacitance. Figure 3.7 models a situation where the substrate contact of the ggNMOSt under test is unique $i.e.$ it does not have any other contact to the substrate. Under such a condition, the

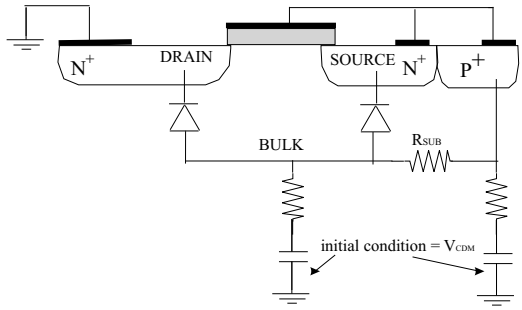


Figure 3.7: Equivalent circuit for CDM, case1.

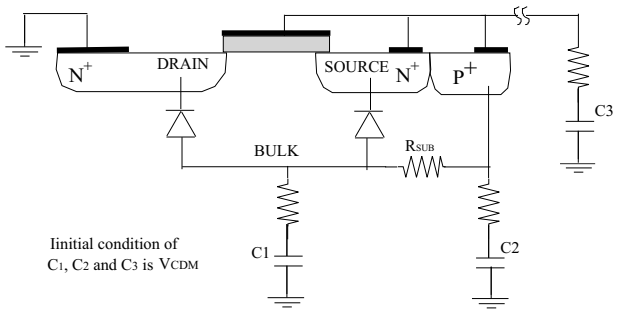


Figure 3.8: Equivalent circuit for CDM, case2.

capacitance associated with the substrate contact is very small and is comparable to that of the drain. Figure 3.9 shows the voltage transient across the device and R_{SUB} when the drain is grounded. As the two capacitors are approximately equal in magnitude, we see that the potential drop across R_{SUB} is much smaller than the knee voltage of the source-bulk junction, needed to turn on the device. Figure 3.8 models the most commonly seen situation where the V_{SS} line shorts all the P^+ substrate contacts in the circuit. Under such a condition, the capacitance associated with the substrate contact is comparable to that of the entire substrate capacitance. When the drain is grounded, the capacitors associated with drain and source discharge. But as the substrate capacitance associated with the source is much larger than that of its drain, the potential drop across R_{SUB} easily exceeds the knee voltage of the source-bulk junction as shown in figure 3.9, and results in the turning on of the device. Thus the behavior of individual protection devices under two pin ESD event can be applied to explain its behavior under CDM stress, provided the substrate contact

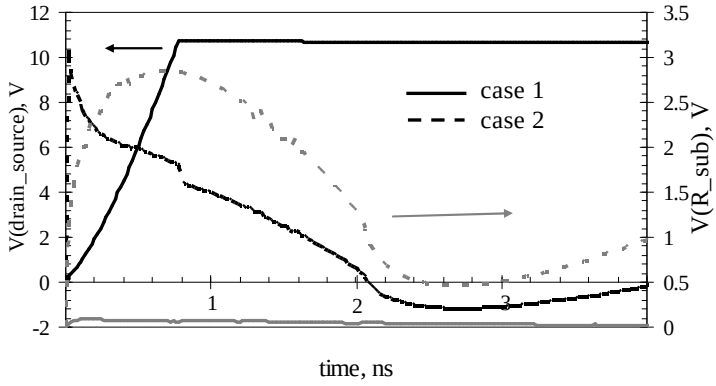


Figure 3.9: Voltage drop across the device and substrate resistance under case1 and case2.

of the protection device under test is well distributed within the circuit and is shorted to its source contact.

3.3 Measurements

Test structures of individual protection devices with varying layout parameters were subjected to field induced CDM stress. Before subjecting them to CDM stress, leakage current[2] measurements were done to ensure that devices don't have failure before being stressed. The samples were CDM tested at different stress levels starting from -200V to a maximum of -2500V in steps of 100V or 200V. After each stress, leakage current measurements are done. An increase of more than 0.1μA in the leakage current was taken as the failure criterion. The corresponding stress level is taken as the failure level.

3.3.1 ggNMOSt

Influence of gate-length

The gate-length of a MOSt determines the transit time of the device and hence the time taken for the device to start conducting [42]. The larger the transit

[2]leakage current - current flowing through the protection device at normal operational condition

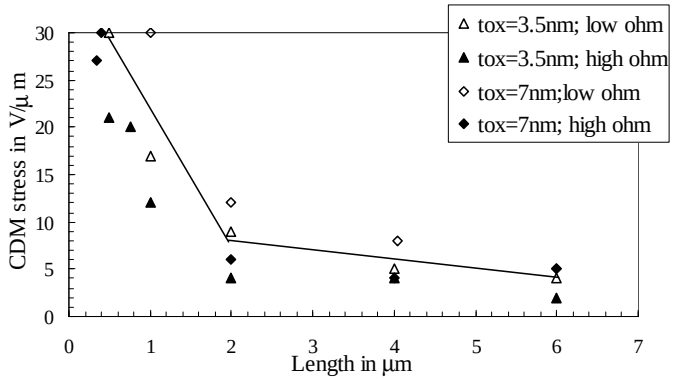


Figure 3.10: CDM threshold level as function of gate length of ggNMOSts.

time, the longer will the drain-bulk junction be in the avalanche breakdown region. If the rise time of the CDM pulse is shorter than the time-on time of the device, all the ESD power will be dissipated at this junction resulting in the burning down of the device. Figure 3.10 shows the CDM threshold level of ggNMOSt in 0.18μm process as function of varying gate-lengths. Also shown is the influence of gate-oxide thickness and substrate resistivity. For effective CDM protection, the protection devices should have a turn-on time faster than the rise time of the CDM pulse [29]. From figure 3.10 we see that devices with gate-length shorter than 1μm can withstand higher CDM stress level, while those with gate-lengths longer than 1μm fail at low stress levels. The rise time of typical CDM current pulse is around 250ps. The transit time of ggNMOSt of 1μm gate-length is also around 250ps [42]. It was shown in [29] that independent of the technology node, all devices with gate-length longer than 1μm showed very good CDM performance. Figure 3.10 also shows that the sensitiveness of the device CDM performance to its gate-length is independent of its gate-oxide thickness and substrate resistivity.

Influence of device width

Device width is related to the amount of ESD current that can be carried by a device without being burnt. The larger the width, the larger is the area of conduction and hence higher should the CDM withstand level be. Figure 3.11 shows the soft failure levels of different ggNMOSTs with $L = 0.18\mu$m as a function of device width, with and without silicide block [29]. The different devices vary in their gate-oxide thickness and substrate resistivity. Figure 3.11

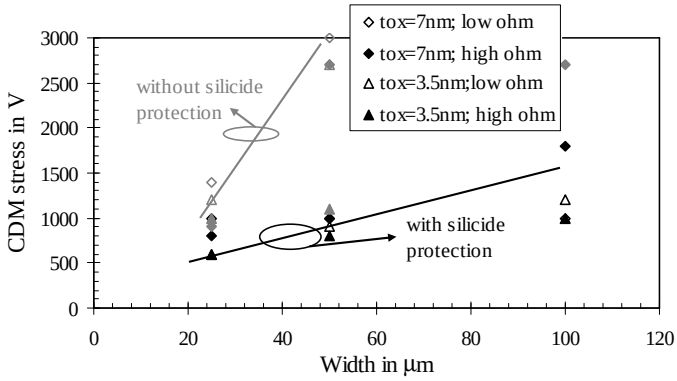


Figure 3.11: CDM threshold level as function of width of ggNMOSts.

shows that devices without silicide block do not scale with its width and have low threshold level as compared to their counterparts with silicide block and this trend holds good for independent of its gate-oxide thickness. The difference in the CDM performance between the silicided and non-silicided devices can be explainable. Silicided region has a low resistivity as compared to silicon and has a lower melting point. As a result the ESD current does not get uniformly spread out through the entire device and current crowding occurs near the junction which in turn reduces the threshold level of the device. For silicide blocked devices, the area which is blocked acts like a ballast resistance. This ensures uniform distribution of ESD current along the whole width of the device and also helps in forcing the current into the substrate region below the drain and avoids current crowding at the drain junction close to the gate edge.

3.3.2 LVTSCRt

Silicon Controlled Rectifier (SCR) is the most efficient of all protection devices because of it very low leakage current during the "OFF" state and low holding voltage during its "ON" state. The layout of a basic SCR along with the parasitic devices which comes into operation during ESD stress is shown in figure 3.13. When the collector/anode is grounded, the collector-base junction of the npn goes into avalanche breakdown generating the electron current in the Nwell which forward biases the emitter-base junction of the pnp. The turn on of the pnp occurs in less than 1ns and this leads to the regenerative $pnpn$ action reducing the overall voltage drop across the device drastically. How-

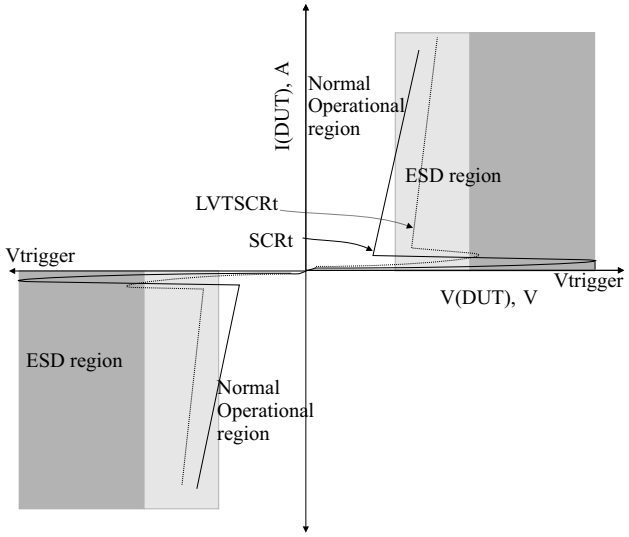


Figure 3.12: *I-V* characteristics of SCRt and LVTSCRt under different regions of operation.

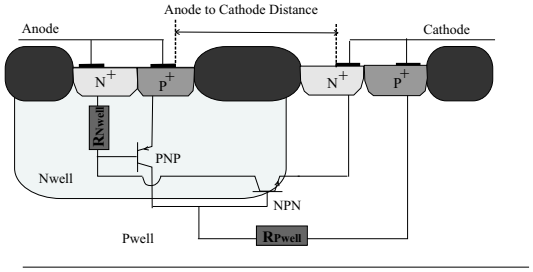


Figure 3.13: Layout of SCRt.

ever the main disadvantage of the SCRt is the very high voltage around 40V to 100V required to turn on the device [1]. This is overcome in the low voltage triggered SCR (LVTSCR) by adding a MOS device with the SCRt as shown in figure 3.14. L-BJT of the MOSt device turns on first, providing avalanche generated hole current in the p-substrate turning on the lateral npn and then the vertical pnp followed by the eventual regenerative SCR action. The *I-V* characteristics of an SCRt and an LVTSCRt is shown in figure 3.12. The turn on voltage level of the SCRt depends greatly on its anode to cathode spacing and the p-substrate resistance. The influence of the anode to cathode spacing

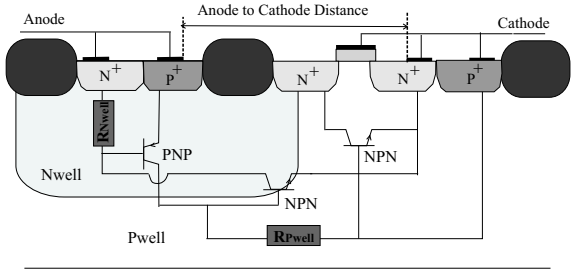


Figure 3.14: Layout of LVTSCR.

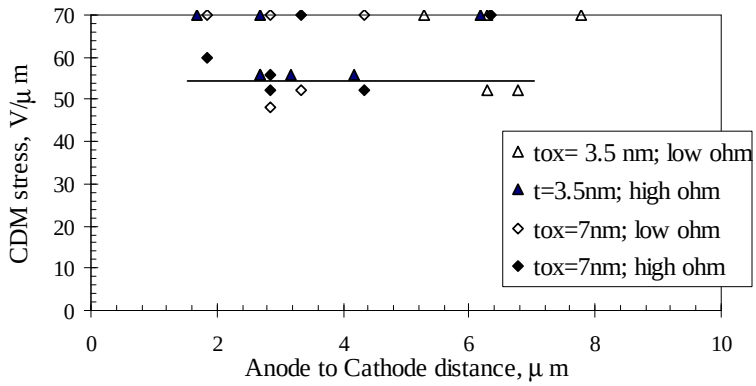


Figure 3.15: CDM performance as function of anode to cathode spacing for a fixed gate-length on LVTSCRts.

and gate-length of the MOS device on the CDM threshold level of individual LVTSCRts is shown in figure 3.15 and figure 3.16 respectively. The variation in the anode to cathode spacing, keeping gate-length constant does not affect the CDM performance of the device. While the gate-length variation makes a significant impact on the CDM performance of the device [29]. This again confirms that the turn-on time of the device is the most dominant parameter that influences the CDM performance of a device.

3.3.3 Failure analysis

Failure analysis done on the failed samples showed thermal failure due to non-uniform conduction of current resulting in soft and hard failure as shown in fig(a) and fig(b) of figure 3.17. ICs that were subjected to higher CDM stress

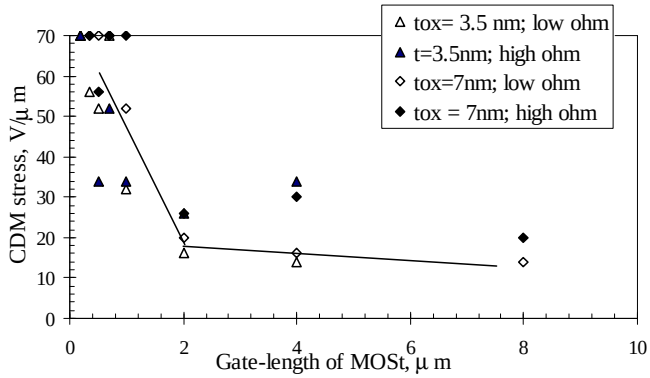


Figure 3.16: CDM performance as function of gate-length of the MOSt in the LVTSCRts.

levels were completely burnt down as shown in figure 3.17-c of figure 3.17 from excess heat dissipation. But gate-oxide failure was not seen in the tested protection devices.

3.4 Simulations

3.4.1 Compact Circuit Model for ggNMOSt

Most of the CDM simulation study is devoted to device simulations [46, 47]. CDM performance of a circuit design does not depend on the behavior of the protection devices alone but on the entire circuit design. Hence circuit simulation is recommended for evaluating CDM performance of a circuit. In this respect, compact circuit model of the protection devices is more useful as it can be directly included in the circuit simulation used to evaluate the CDM performance of the circuit [48]. The most used compact circuit model for ggNMOSt is shown in figure 3.18. This is basically the Ebers Moll model with an additional avalanche current source added to account for the high current behavior of the device. The diode currents through the drain base junction and the source base junction is represented by I_{DB} and I_{SB} respectively, are given by,

$$I_{\mathrm{DB}} = IS_{\mathrm{DB}}.[exp(V_{\mathrm{DB}}/Ut) - 1] \tag{3.4}$$

$$I_{\mathrm{SB}} = IS_{\mathrm{SB}}.[exp(V_{\mathrm{SB}}/Ut) - 1] \tag{3.5}$$

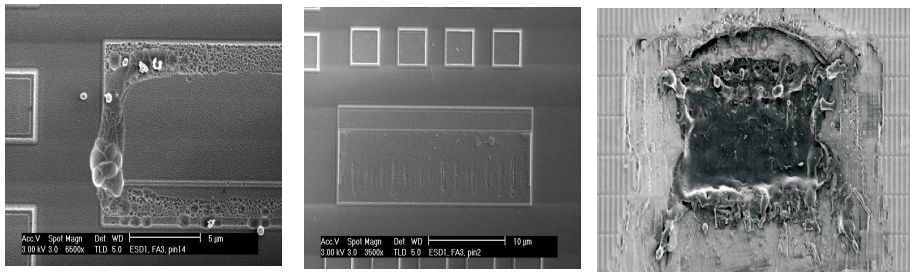


Fig (a) Fig (b) Fig (c)

Figure 3.17: SEM pictures of ggNMOSts after CDM stress showing different kind of failures. Fig(a)A short resulting from a non-uniform conduction of discharge current (hard failure), Fig(b)Needle shaped extrusions from the melting of silicon resulting in leakage current increase (soft failure), Fig(c)An open from excess heat dissipation resulting in the melting of silicon along with the metal layers above it.

Because of the symmetry in the device $i.e.$ both the drain and source can be interchanged, IS_{DB} = IS_{SB} = IS. The emitter, I_2 and collector, I_3 currents flowing into the base together comprise the transistor current and is given by,

$$I_2 = \alpha_{\mathrm{R}}.I_{\mathrm{DB}} \tag{3.6}$$

$$I_3 = \alpha_{\mathrm{F}}.I_{\mathrm{DB}} \tag{3.7}$$

α_{R} = α_{F} = α, because of symmetry in the device. The current gain, β in the transistor is generally low and for simplicity it is assumed to be 10.

$$\alpha = 1/(1+\beta) \tag{3.8}$$

The avalanche current source is given by

$$I_{\mathrm{AVC}} = (M-1).I_{\mathrm{SB}} \tag{3.9}$$

where the multiplication factor M is given by,

$$M = 1/[1-(V_{\mathrm{DB}}/V_{\mathrm{BV}})^{n1}] \tag{3.10}$$

where V_{BV} is the breakdown voltage of the collector base junction and n1 an empirical constant whose value ranges from 2 to 4 typically. But in our simulations we have taken n1 = 1 from our experimental observation. This is done in order to model the lowering of the snapback voltage because of the dV/dt triggering during fast rise time stress. I_{AVC} gets turned on only when both the

multiplication factor and the current through the diode D_{SB} are relevant. Once the current source I_{AVC} gets turned on, the potential across the collector base junction is determined by I_{AVC} and not by the diode D_{DB}. The potential across this junction drops until equilibrium is reached. Applying Kirchoff's current law,

$$I_{\text{DB}} + I_3 + I_{\text{AVC}} = I_{\text{BE}} + I_2 \tag{3.11}$$

Substituting their respective values, we get

$$V_{\text{DB}} = V_{\text{BV}}[(\beta/(2\beta+1))^{1/n1)}] \tag{3.12}$$

Both the depletion and diffusion capacitance are taken into consideration in the model. The majority carriers near the edges of the depletion region move as the depletion region expands or contracts in response to a changing reverse bias resulting in charge storage. This charge storage is modelled by a depletion capacitance.

$$C_{\text{depl}} = dQ/dV \tag{3.13}$$

Depletion capacitance plays a significant role depending on the rise time of ESD stress events. The observations show that as the rise time of the TLP stress is decreased, the devices get turned on before the breakdown potential is reached [21, 42]. This is because the displacement current from the junction capacitance was large enough to cause the voltage drop across source-bulk junction diode to be forward biased and thus helps to turn on the device even before the junction breakdown voltage is reached.

The variation of stored minority carrier charge in the quasi-neutral regions under forward bias is modelled by another capacitance known as the diffusion capacitance. The amount of stored charge is given by,

$$Q_{\text{diff}} = tt.I_{\text{d}} \tag{3.14}$$

where,
I_{d} - drain current flowing through the junction
tt - transit time represents the mean life time of the injected minority carriers in the case of long diodes or the time duration of the minority carriers in the neutral region of a short diode. In the case a ggNMOSt, tt is the time taken for the injected electrons from the emitter to reach the collector and hence a function of its effective channel length [42]

$$tt = L^2/(4.D_{\text{n}}) \tag{3.15}$$

where, D_{n} is the diffusion constant and L, gate-length of the MOSt or base length of the parasitic L-BJT. Gate-length is of paramount importance in the

case of CDM like stress event, where the turn-on time of the device plays a significant role. Equation 3.15 assumes that the entire source-bulk junction contributes to I_{d}. But in reality, during the initial turn-on time, only that portion close to the intrinsic base region $i.e.$ the side wall of the source region close to the base would actively contribute to the transistor current and this would effectively slow down the transit time. The correction factor introduced by Krieger [49] to estimate this slowed down transit time is given by,

$$tt' = K_{\mathrm{G}}.L^2/(4.D_{\mathrm{n}}) \tag{3.16}$$

where, K_{G} is the "Kreiger factor". K_{G} is an estimation of the ratio of electron injection into the base region and stray electron injection under the bottom layer of the source. The value of KG is found to be KG $\approx$ 3.2 for practical reasons [42].

The other parasitic path which begins to conduct when the drain is subjected to negative ESD stress is the diode formed by the drain-bulk junction as shown in figure 3.18. R_{BULK} is the bulk resistance between the drain and substrate. At high current injections, the effective value of R_{BULK} decreases due to conductivity modulation. This effect is taken into account by modelling R_{BULK} as current dependent resistor,

$$R_{\mathrm{BULK}} = 1/(1 + 10.I_{\mathrm{d}}) \tag{3.17}$$

This model has been tested on stability in extreme CDM transients of 2000V/ns. But however this model does not take into account the thermal effects of the ESD current.

3.4.2 Model Validation from TLP and vf-TLP

Having built a circuit model, we would like to know whether this model can mimic the sensitiveness of the protection device to rise time of the CDM pulses and the influence of its layout parameters on its device behavior. As we do not have any direct *I-V* measurements of the device behavior under CDM stress, we use Transmission Line Pulse (TLP) and very fast TLP (vf-TLP) measurements to check the validity of our model. During a TLP measurement, the device is subjected to voltage pulses with rise time 10ns and 100ns pulse width. The amplitude of the pulse is incremented in a sequential manner until the device fails. For each voltage stress level, the voltage across the device under test V_{DUT} and the current through the device under test I_{DUT} is measured at around 80ns. This procedure is repeated until the device fails or until the maximum

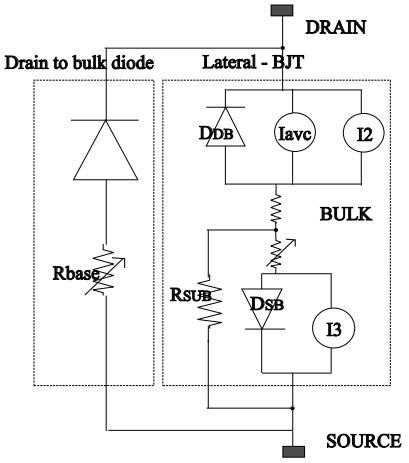


Figure 3.18: Compact circuit model for ggNMOSt.

stress level is reached. At the end of the measurements, *I-V* characteristic of the device under TLP stress is obtained. The same procedure is followed in the simulation environment and the *I-V* curve under TLP is obtained. Figure 3.19 shows the measured and simulated *I-V* curve under TLP. We do see a fairly good agreement of the measured and simulated curves. One reason for the large discrepancy at higher stress level can be from thermal effects which are not taken into account in the simulation. As the CDM performance of a de-

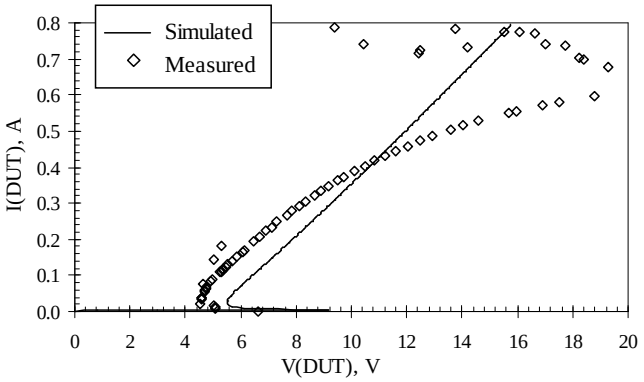


Figure 3.19: Measured and simulated *I-V* transients across ggNMOSt (L= 0.18μm, W= 50μm, Si_prot= 6μm) during TLP measurements.

vice depends on the switching transients of the device, it is important to check whether the simulation can model the transients of the device as well. The measured and simulated voltage transients of the device under TLP stress show that the protection device simulated turns on faster than the measurements. The observed slower transient could be simply because the actual current pulse as seen by the device is slower than what is thought to be applied because of the tester parasitics. Figure 3.20 shows the I-V transient across the device during different TLP stress levels. From figure 3.20 we see the ringing of TLP pulses and voltage across the device to exceed much higher than the turn-on voltage of the device observed during the transient measurements indicating a strong influence of the parasitic inductance and capacitance of the test set-up on the measurements. On including the parasitic components of the tester in our simulations, we could simulate the same effects as seen during measurements as shown in figure 3.21. But as the values used for the simulations were only rough estimates, we could not get an exact fit between the measured and simulated results. Figure 3.22 shows the *I-V* characteristic of ggNMOSts for varying gate-lengths. We see that as the gate-length is increased, the amount of snapback experienced is decreased. That is the holding voltage of the device gets increased from 4V to 10V as the gate-length increases from 0.18μm to 6μm. This variation in the *I-V* characteristics of the protection devices with varying gate-lengths is also found in the simulated results as shown in figure 3.23. The behavior of the protection device also varies with the rise time of the ESD pulse. Figure 3.24 shows the initial *I-V* transients across a ggNMOSt when subjected to a TLP of t_{rise} = 10ns and a vf-TLP of t_{rise} = 5ns. With faster rise time of the ESD pulse the drain-bulk junction capacitive current increases and provides a leakage current. As a result even before the drain-bulk junction reaches its breakdown voltage, the source-bulk junction gets forward biased and the device turns on. As the device is not in the deep breakdown region, the voltage snapback observed across the device is reduced. Thus with a faster rise time ESD pulse, we see a lower trigger voltage and less snapback. This is also seen from the simulated results plotted in the same figure. Although the simulated and measured TLP transients did not match, the trend in the variation of I-V with the layout parameters and the rise time of the pulse matches very well between the simulations and measurements. We use this model to simulate the behavior of the protection device in the full chip circuit model of the IC, where a very accurate model is not the criterion but a model which emulate the sensitiveness of the device behavior to the rise time of the ESD pulse and its layout parameters.

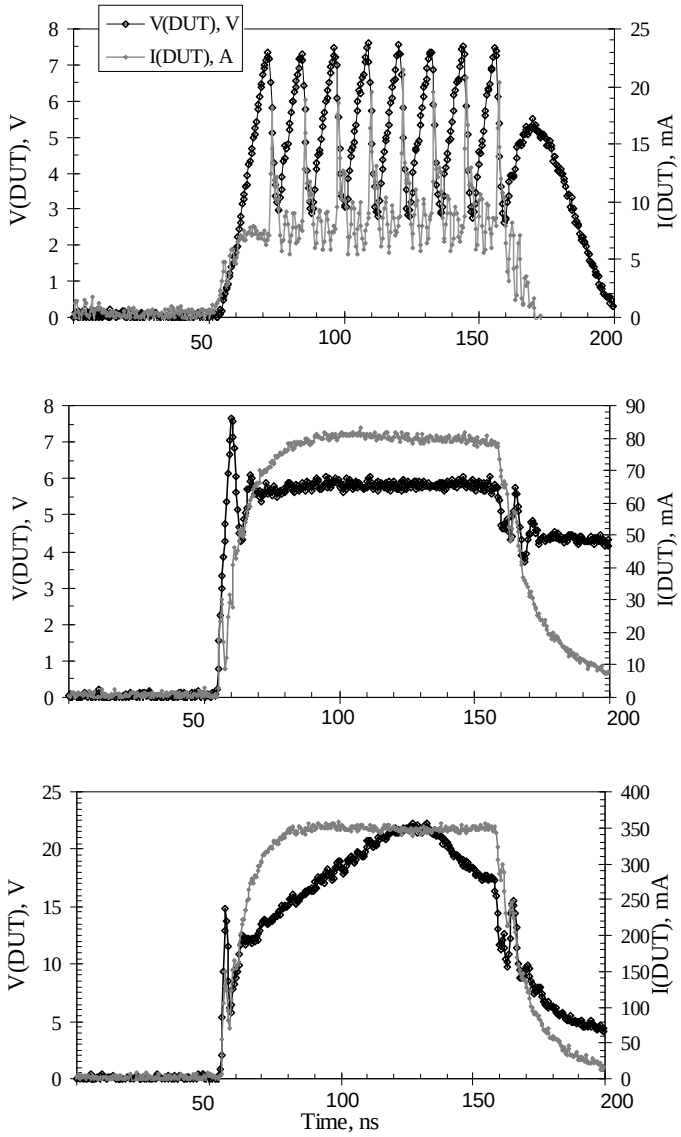


Figure 3.20: Voltage and current transients across the device during 40V, 150V and 580V TLP stress measurements.

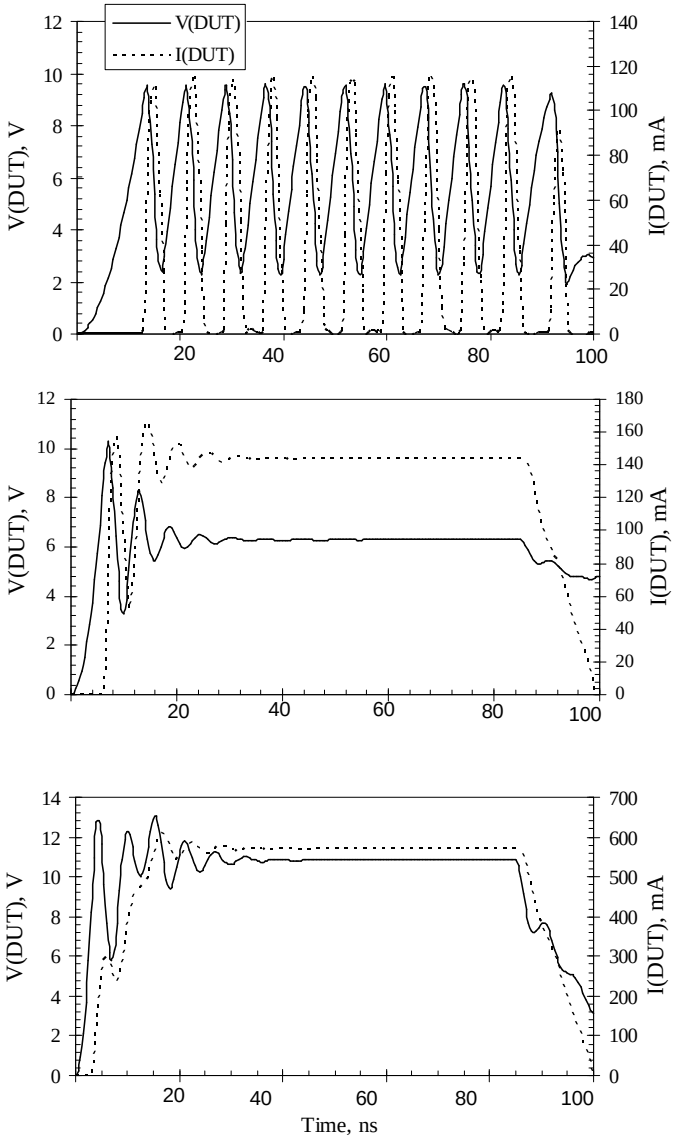


Figure 3.21: Voltage and current transients across the device during 40V, 150V and 580V TLP stress simulations.

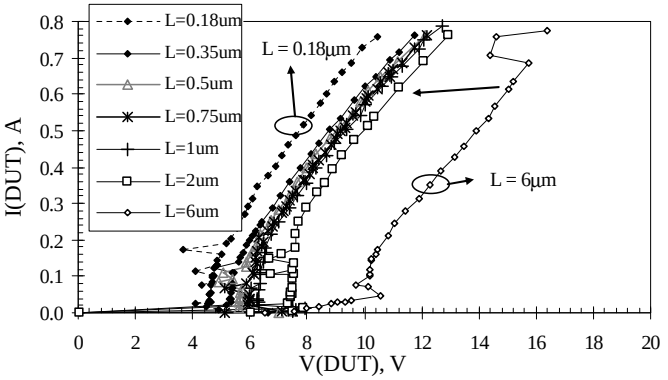


Figure 3.22: Influence of gate-length variation on the I-V characteristics during TLP measurements.

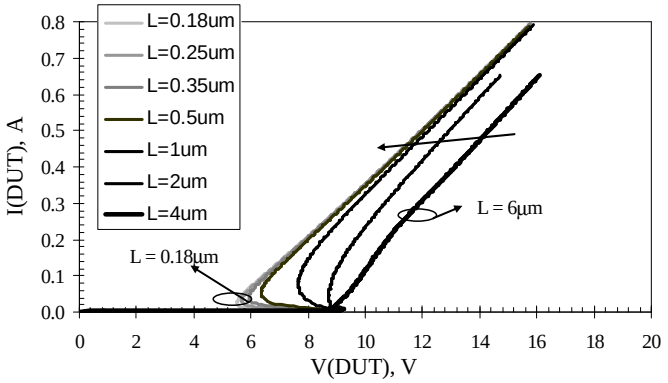


Figure 3.23: Influence of gate-length variation on the I-V characteristics during TLP simulations.

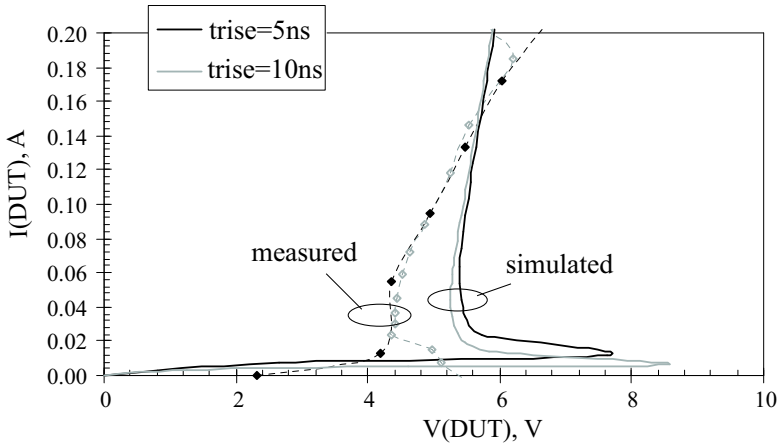


Figure 3.24: Influence of rise time variation on the I-V characteristics during TLP and vf-TLP measurements and simulations.

3.4.3 Compact Model of MOSt

The model in section 3.4.1 describes the behavior of the parasitic devices that become active when a grounded gate MOS transistor is subjected to under high current transients. Mergens [48] had shown that by including a MOSt in parallel to the compact transistor model as shown in figure 3.25, the same model can be used for both normal operational region and at ESD conditions. This model also helps in modelling the gate-coupling effect on the voltage transients across the MOSts. The MOSt model used in our simulation is the standard model available to model the device behavior under its normal operational conditions. The bulk node of the MOSt model is connected to the base of the ggNMOSt and hence coupled to the gate of the MOSt through the gate-oxide capacitor. This is to include the gate-coupling effect on the high current behavior of the MOSt. The gate voltage plays a significant role in determining the turn on voltage of the device.

3.5 Conclusions

CDM measurements on different types of protection devices show that the protection devices with turn on time shorter than the rise time of the CDM pulse and having a uniform distribution of ESD current throughout the device

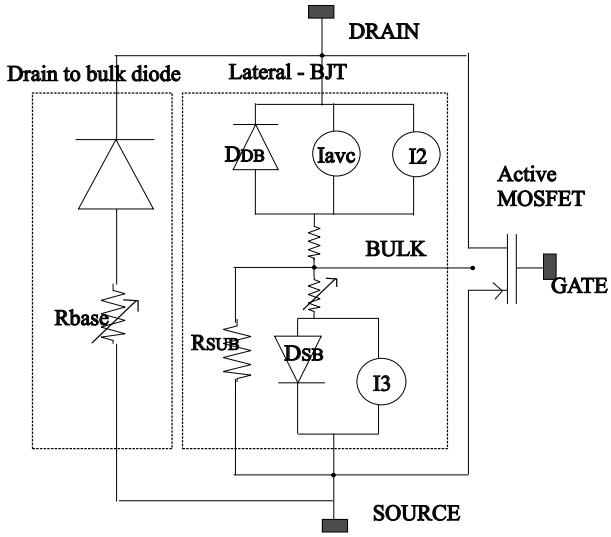


Figure 3.25: Compact transistor model with MOSt.

width are the best candidates for CDM protection. The simulation models available for a two pin high current event can be applied to model the CDM behavior of the devices provided the substrate contacts are well distributed and are connected to the source of the protection device. A compact circuit model that can simulate the high current transient behavior of MOSt is built in the SPECTRE simulator.

4 Chapter I/O Protection Circuits

Having studied the criteria for a CDM robust protection device, our next step is to build them efficiently into the protection circuit design. The input and output (I/O) buffers which form the intermediate link between the external world and the internal circuitry are vulnerable locations of CDM failure. Hence making robust I/O protection circuits is very important. The general available I/O protection designs and the CDM requirements for a robust design are briefed. Few design parameters which are believed to influence the CDM performance are studied from CDM measurements and simulations.

4.1 Introduction

The first portion of the core circuit which forms a link between the outside world and the internal circuit are the input and output buffers. Therefore these are the locations which will be subjected to maximum ESD stress. Hence a large deal of ESD protection design has been focussed on protecting these locations [43], [41]. One of the main criteria for achieving a good CDM robust I/O protection design is to avoid voltage drop across the gate-oxide of the MOSt in this circuit to exceed its breakdown voltage.

In this chapter, the generally available I/O protection design in pad based protection and the role of each of the design parameters in influencing the voltage transients across the gate-oxide of the MOSt at the input and output buffers is briefed. Later, CDM measurement results done on a test structure with varying protection design built in a 0.6μm CMOS technology node are discussed. The measurement results are explained with 2D CDM circuit simulation and the

design variations which can enhance the CDM performance of the protection design is studied. The efficiency of the protection designs are discussed under the assumption that the power lines V_{DD} and V_{SS} are well coupled to the substrate capacitance. This assumption is not wrong because the V_{DD} and V_{SS} lines are directly connected to their respective substrate contacts.

4.1.1 Input Protection Design

General protection design at the input pad is as shown in figure 4.1. Each input pad is connected to the supply lines via large protection devices protection devices also known as primary protection devices. Apart from these primary protection devices, a decoupling resistor between the input pad and the circuit to be protected is a general recommendation for ESD protection. Sometimes there is an additional protection device closer to the circuit to be protected as shown in figure 4.1 connected across the gate-oxide to be protected.

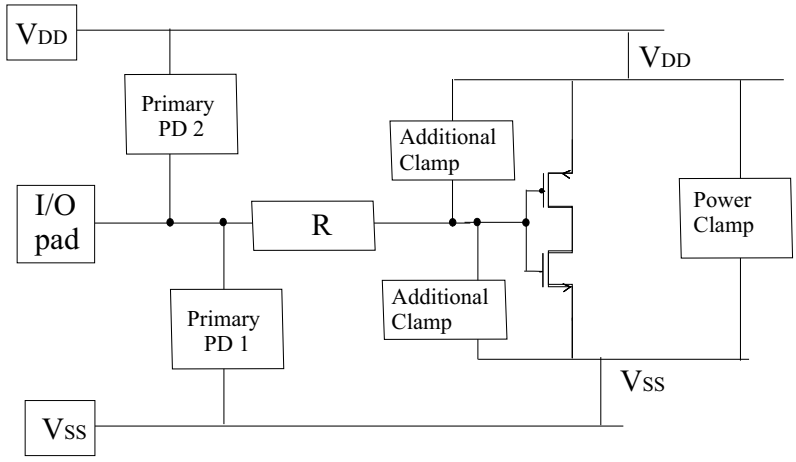


Figure 4.1: Input Protection design.

Role of Decoupling Resistor

Presence of a large resistor *R*, between the protection device and the circuit to be protected as shown in figure 4.1, helps to limit the amount of discharge current flowing into the internal circuitry under "Classic ESD" (HBM, MM)

stress. In the case of CDM stress, it has an additional role to play. The decoupling resistor R in combination with C_{gate}, creates an RC delay to the CDM pulse as seen by the gate (See figure 4.2). That is, the gate sees the CDM pulse with a delayed rise time as compared to its pad. The effect of this delay on the voltage drop seen across the gate-oxide is explained in the figure 4.3. If V_{pad} be the potential at the pad then the voltage across the gate will be given by,

$$V_{\text{gate}} = V_{\text{pad}} - \Delta V \tag{4.1}$$

$$= V_{\text{pad}} - (dV/dt).RC \tag{4.2}$$

where, dV/dt is the slope of the CDM transient. Thus the gate potential will be lesser than the potential at the pad depending on the RC delay time and the slope of the current transient.

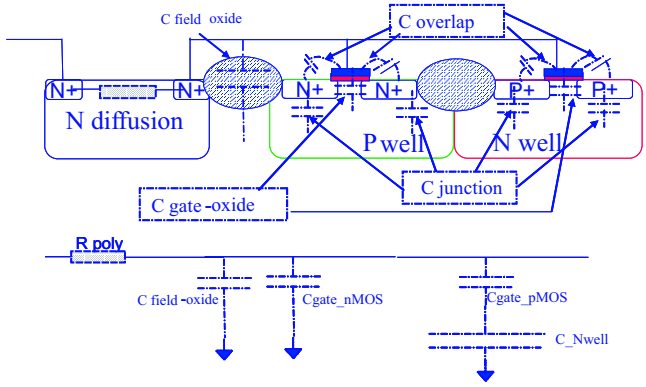


Figure 4.2: Parasitic gate capacitance associated with the substrate.

Another way of looking at the same situation is to see two discharge paths available, one through the protection device and second through the gate and decoupling resistor. Before the protection device turns on, the amount of current flowing through the first path is the junction capacitance leakage current and that through the second path is the gate leakage current. The larger the gate capacitance, the larger would be the current through the second path and hence the higher the potential drop across R. This indicates that the gate voltage is lower than at the pad by an amount equal to the voltage drop across R. Once the protection device turns on, most of the discharge current gets diverted into the protection device and the current through the second path is reduced drastically close to zero and the gate and pad is brought to the same potential. Thus the RC delay helps in guarding the gate potential only until the protection device turns on.

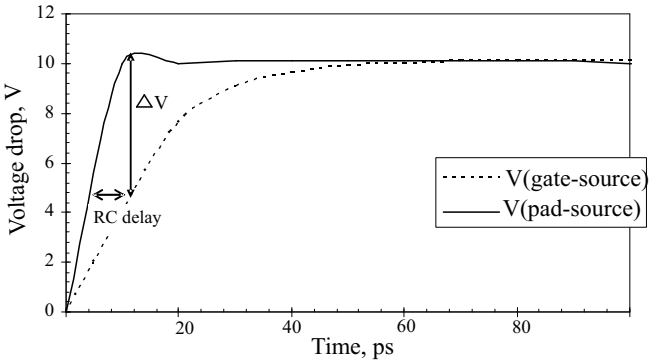


Figure 4.3: Voltage transients as seen by the discharged pad and the gate with respect to the source during CDM pulse. $R = 100\Omega$, $C = 100$fF.

While designing a protection circuit, one should be careful not to hamper the normal operation of the circuit. The value of the decoupling resistor limits the maximum operational speed of the circuit. Also the effective value of R can be less than the intended value, because of the parasitic contacts which the resistor makes with the substrate [50]. With larger dimensions of R, the effective value of R gets decreased drastically because of its parasitic contact with the substrate. Hence one should be aware of this fact while designing a protection circuit.

Role of Added Clamp

Figure 4.1 shows an ideal protection design where the parasitic resistance of the power lines are not included. But in reality the bus lines have a non-zero resistance. The actual schematic sketch of an input protection design along with its parasitic elements and the CDM current source as seen by the circuit is shown in figure 4.4. The source of the protection device is not directly connected to the power lines to avoid external disturbances at the input pad to be seen at the internal circuit. One design aspect worth noting is that the connection between the V_{SS} line and the source of the protection device is done in the first metal layer whose effective metal line resistance, represented by R_{BUS} in figure 4.4 is much larger than the V_{SS} sheet resistance. The same holds for the V_{DD} line. The discharge current flowing through the circuit when subjected to a negative CDM stress, is shown by the arrow mark in the figure 4.4. From the figure 4.4 we see that the voltage drop seen across gate-oxide of the MOS tran-

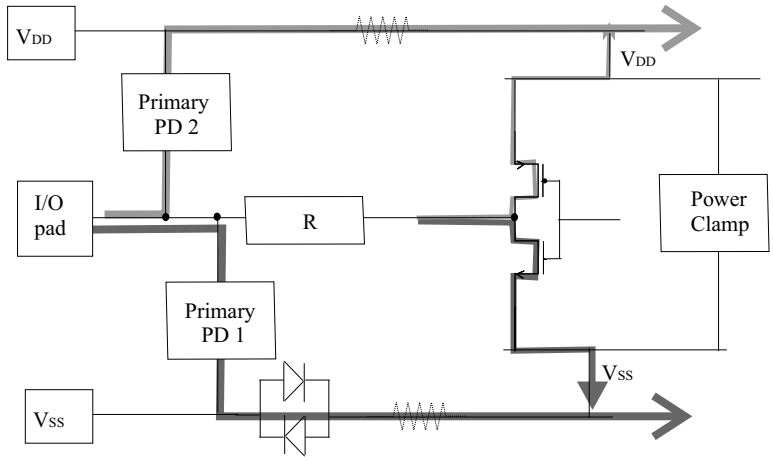


Figure 4.4: Input protection design along with the parasitic bus line resistance and discharge path through the circuit.

sistors in the input inverter is equal to the voltage drop across the corresponding protection device plus the voltage drop across the bus line. The protection device to the V_{DD} acts as forward biased diode while the protection device to the V_{SS} line acts in its snapback mode. Thus during negative CDM stress the maximum voltage drop is across the NMOS in the I/O buffer. Therefore the entire discussion is focussed on the voltage and current transients across the NMOS. The same holds good for PMOS under positive CDM stress. Placement of a protection device close to the gate-oxide to be protected and clamping them across the same supply rails as the protected device, does not allow the voltage seen across the gate-source to increase beyond the holding voltage of the clamping device. But the added clamping devices being placed closer to the core circuitry has a limitation on its device width and hence the amount of discharge current handled by it is very much limited.

The presence of decoupling resistor limits the amount of current flowing through the added clamp. Once the primary protection turns on, most of the discharge current is diverted into the primary protection and the current through the clamping device gets drastically reduced. Henceforth, the function of the added clamp is to ensure that the potential across the gate does not exceed its clamping voltage. The general property of a primary protection device, is that it can handle large current, but has slower turn on time. Hence it would be ideal if the clamping device added closer to the device to be protected is faster than the primary protection. The addition of clamping device with faster turn-on

time would then ensure that the potential drop across gate-oxide of the MOS does not exceed its clamping voltage both before and after the turn-on of the primary protection. In combination with the decoupling resistor, the current flowing through the added clamp would be limited. Thus the combination of added clamp with decoupling resistor will improve the CDM performance of the protection design to a great extend.

4.1.2 Output Protection Design

The general protection design at an output buffer is as shown in figure 4.5. The figure also shows the current flowing through the circuit under a negative CDM stress. In the case of output buffer, it is not the gate-oxide voltage transients which causes the failure, but the amount ESD current flowing through the MOS in the output buffer. One may expect gate-oxide failure from voltage overshoot across drain and gate, when the gate is shorted to its source. But this is the configuration in which any protection device works. In fact this property is made use of in some protection networks where the dimensions of the output buffer is intentionally made large enough to handle ESD currents. In other words, the output buffer itself also acts as a protection device. But if the MOS transistors at the output buffer are of very small size then it cannot handle the ESD current and we need extra protection circuit which is the scenario which will be studied in this chapter. For a robust output protection design, the current

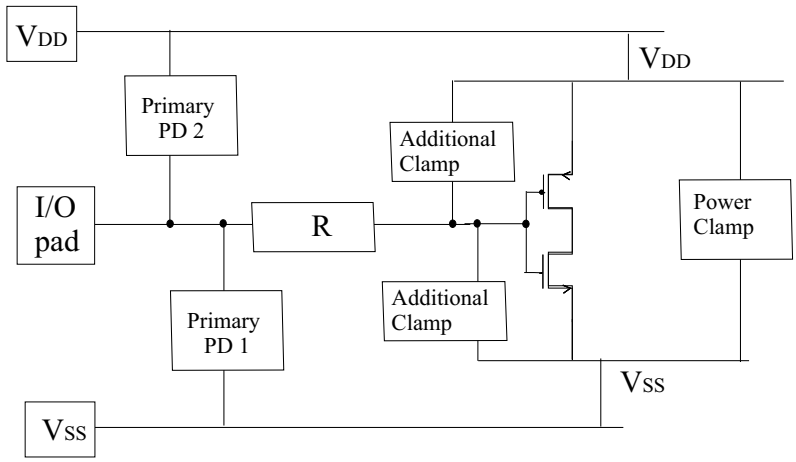


Figure 4.5: Output protection design

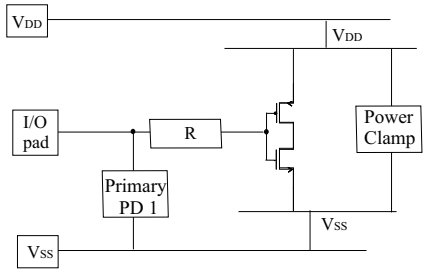


Figure 4.6: Input protection design.

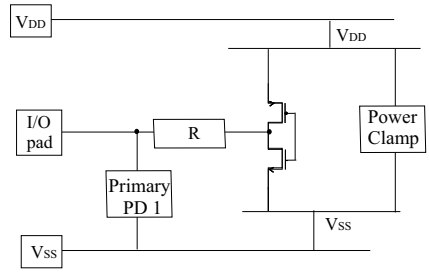


Figure 4.7: Output protection design.

flowing through the MOS in the output buffer should be kept low. This can be achieved by:

1. Making the gate-length of MOS in the output buffer longer than the protection device, thus slowing down the turn on of the MOS.
2. Increasing the value of decoupling resistor so as to limit the ESD current flowing through the MOS in the output buffer.

4.2 Measurements

4.2.1 Description of test structure

A test structure with varying I/O protection designs were made in the 0.6μm technology node and their CDM performances were studied. Figure 4.6 and figure 4.7 shows the schematic sketch of the input and output protection structure studied. The various design variations studied are listed in the table 4.1.

Table 4.1: Design parameters of the various input protection structure studied. The dimensions of the protection devices (both pad clamp and power clamp) were W/L = 100/0.6

	Poly Resistor [Ω]	Dimensions of MOSt to be protected [W/L]
Input buffer	0,10,50,100,200,500	0.75/0.6
Output buffer	0,10,20,50	0.75/0.6
Output buffer	0	1/1, 1/1.2, 1/1.5, 1/2

4.2.2 CDM Stress and Failure Diagnosis

The I/O pins of the test structure were subjected to field induced CDM stress starting at -200V to -1000V in steps of 50 or 100. After each stress, leakage current through the I/O pin was measured when the V_{DD} and V_{SS} supply lines were at 5V and 0V respectively. The leakage current measurements were done with the I/O line at three different levels namely 0V, 2.5V and 5V. An increase of 0.01μA in the leakage current was taken as the failure criterion. The CDM stress level of the corresponding stress was taken as the CDM failure level. Each measurements were repeated for three samples. Table 4.2 shows the possible failure locations when the leakage current increases at various voltage levels of the I/O pad. Earlier CDM measurements on individual protection

Table 4.2: Possible failure locations at various voltage levels of the I/O pad.

Voltage at I/O pad [V]	Clamp to V_{SS}	NMOS at the I/O buffer	PMOS at the I/O buffer
0		Fail	
2.5	Fail	Fail	Fail
5	Fail		Fail

device with the same dimensions as used in the I/O protection design, did not fail after -2000V CDM stress. Hence the possibility of failure at the protection device itself was ruled out.

4.2.3 Results and Discussions

Poly resistance variation in input protection design:

The role of poly resistance is to slow down the transients as seen by the gate-oxide of the MOS in the input buffer. Figure 4.8 shows that the failure levels diagnosed at 0V and 2.5V agree with each other quite well. This brings us to conclude that the first failure location was always at the PMOS of the input inverter. Also we see the failure level to be independent of the poly resistance value. When subjected to higher stress levels, we do see a gate-oxide failure at the NMOS also.

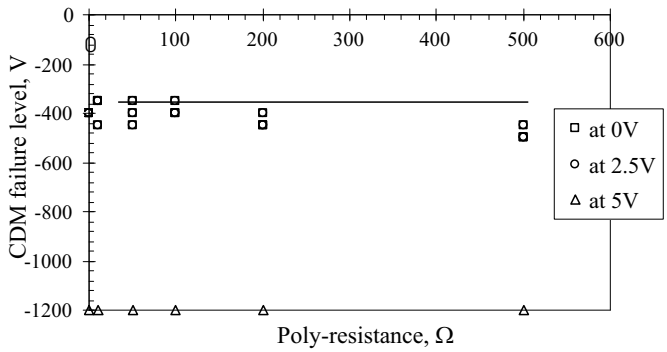


Figure 4.8: Influence of poly resistance in the CDM failure level of input protection design used in the test structure.

Poly resistance variation in output protection design:

The MOS transistors in the output buffer is in the grounded gate configuration and hence would act as clamping devices, conducting the ESD current through it. But as these devices are very small in size (only 1/100th of the protection device) they cannot handle a sufficiently large current. With increase in poly resistance we expect an improved performance of the protection design as the resistor would limit the amount of current flowing through the MOS transistors in the output buffer. Figure 4.9 shows CDM failure level diagnosed at different voltage levels (0V, 2.5V and 5V) at the output pad. From the figure we also see that it is NMOS that fails first. Figure 4.9 shows a noticeable improvement in the CDM robustness from -300V to no fail as the poly-resistance is increased to 20Ω. As the measurements were stopped at -1000V CDM stress, we do not know if there is a saturation in the failure level with increase in resistor. With respect to the PMOS, increase in poly-resistor would mean increase in the series resistance of its parasitic diode. The increase in the resistor decreases the amount of current flowing into the grounded pin through the PMOS in the output buffer. From figure 4.9, we see improvement in the failure level of PMOS with increase in poly resistance.

Gate-length variation of output buffer:

Gate-length plays a major role in deciding the switching speed of the parasitic Bipolar Junction Transistor (BJT) in a ggMOSt. The longer the gate-length

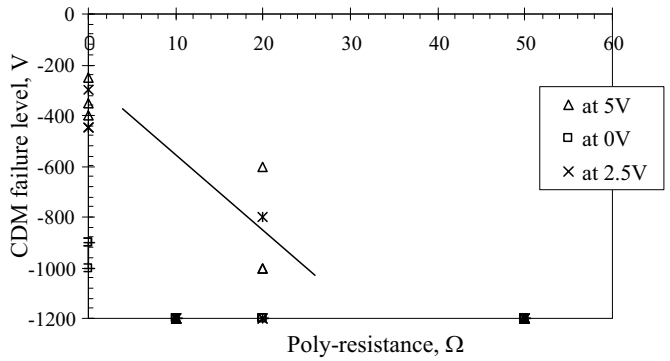


Figure 4.9: Influence of poly resistance in the CDM failure level of output protection design used in the test structure.

of the MOSt, the longer is the time taken for the turn on of these devices. When the gate-length of the MOSt at the output buffer is made longer than the primary protection (protection device at the pad), the MOSt in the output buffer would switch on slower. As a result most of the CDM current will be conducted through the primary and thus enhances the CDM performance of the output protection design. The test results as shown in figure 4.10 ascertains our reasoning.

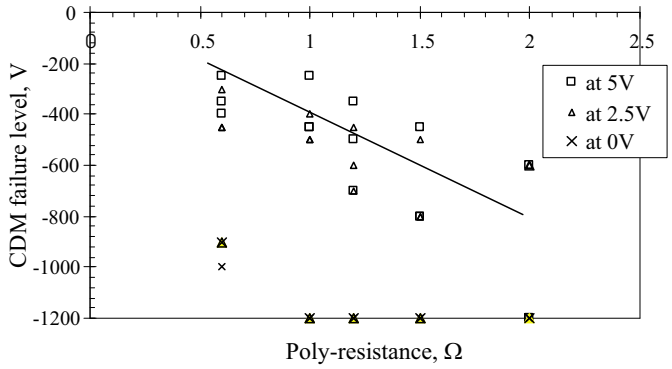
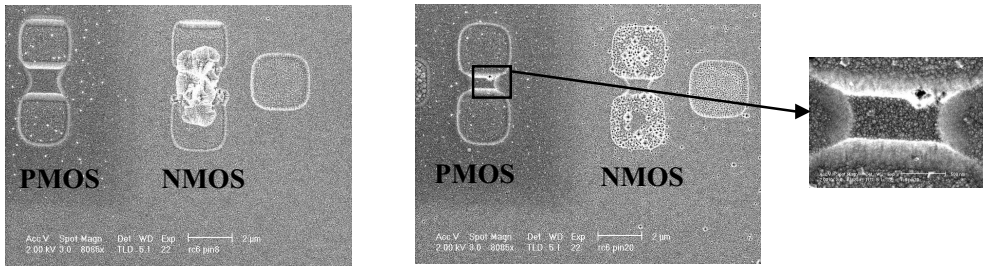


Figure 4.10: Influence of gate-length of MOSt in the output buffer on the CDM failure level of output protection design.

4.2.4 Failure Analysis

Extensive failure analysis of the failed samples was carried out to confirm our line of reasoning on the failure location and the type of failure. In order to confirm if the failure was really from gate-oxide breakdown, failure analysis was done in different ways.

1. Samples were de-processed using hydrofluoric acid and SEM pictures of the devices were taken. The failure location on the input buffer was invariably at the PMOS and they were all gate-oxide failures as shown in figure 4.11. In the case of output cells, the failure was from thermal breakdown at the NMOSt of the output buffer.

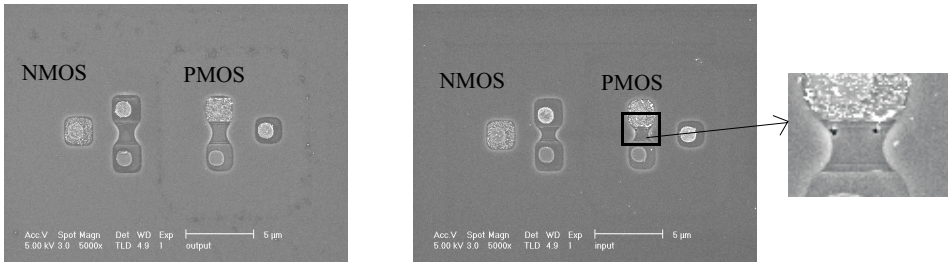


Output buffer Input buffer

Figure 4.11: SEM pictures taken at the I/O buffers after removing the metal and oxide layers.

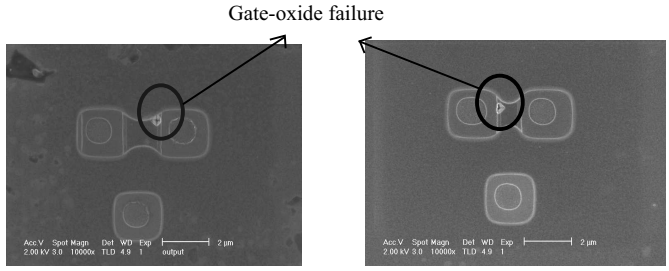
2. Silicon was removed from the backside by polishing and etching, leaving only oxides between the silicon and the metal layer. SEM pictures were then taken from the backside (See figure 4.12). Gate-oxide fails if present are shown as dark spots in the gate-oxide region. The SEM pictures showed gate-oxide failures at the input buffer while no oxide failures at the output buffers, which is in accordance with our reasoning.

3. Silicon was further etched close to the gate-oxide and SEM pictures were taken from the top side. Figure 4.13 shows the SEM pictures taken at the input and output protection buffer. In contrast to the observations earlier, the gate-oxide failure was seen at the output buffer as well. It is quite possible that a gate-oxide like failure can be seen from drain to source breakdown.



Output buffer Input buffer

Figure 4.12: SEM pictures taken at the I/O buffers from the backside of the wafer after polishing off the silicon.



NMOS at Output buffer PMOS at input buffer

Figure 4.13: SEM pictures taken at the I/O buffers from the topside of the wafer after polishing off the silicon.

General observation from the failure analysis made on the failed samples showed gate-oxide failure of PMOS at the input inverter and thermal breakdown of NMOS at the output buffer. The failure location from the electrical measurements and the failure analysis coincide with each other.

Conclusions:

The CDM test results on the test structures of input and output cells show an overall improved performance of the output buffers as compared to input buffers. Lack of dedicated protection device to the V_{DD} line could have resulted in the early gate-oxide breakdown of the PMOS transistor in the input buffer. As a result, we could not study the role of poly resistance on the CDM performance of the input cells. In the case of output cells, we see a signif-

icant improvement with increase in decoupling resistor. The increase in the gate-length of MOS transistors in the output buffer improves the CDM performance of the output cell. But as the over all performance of the output cells were higher, we have only few devices showing failure. From the CDM measurements on the test structures, we could not draw any strong conclusions on the effect of decoupling resistance variation on the CDM robustness of the circuit. Hence we use CDM simulation to study the effects of these protection design variations on the voltage transients across the device.

4.3 Simulations

In order to simulate the current voltage transients across a circuit during CDM stress, it is absolutely necessary to model the CDM current source and its discharge path through the circuit. The circuit in the test structure is very simple with only two bus lines V_{DD} and V_{SS}, apart from each pad line. The V_{DD} and V_{SS} lines make very good contact with the C_{SUB}, which is the major CDM current source. Each of the MOS at the input and output buffer has separate substrate contacts, which are shorted to the source. Hence the risk of gate-substrate voltage is not present in the design.

The following analysis on different protection designs are done with the assumption that all the CDM current from C_{SUB} is flowing into the grounded through the V_{DD} and V_{SS} lines. The circuit used to study the CDM performance of a circuit is shown in figure 4.14. The CDM current sources are modelled by the pre-charged capacitors C_1 and C_2 which represent the C_{SUB} coupled with the V_{SS} and V_{DD} line respectively.

4.3.1 Input Protection Design

In the analysis presented, we start with the protection design used in the test structure and later study the influence of design parameters in the voltage transients seen across the gate-oxide of the MOSt in the input buffer. (As the source and substrate nodes are shorted, voltage transients across gate-oxide refers to the voltage transients across gate and source nodes.) The aim of this simulation analysis is to study the influence of various design parameters on the voltage transients across the gate-oxide in the input buffer.

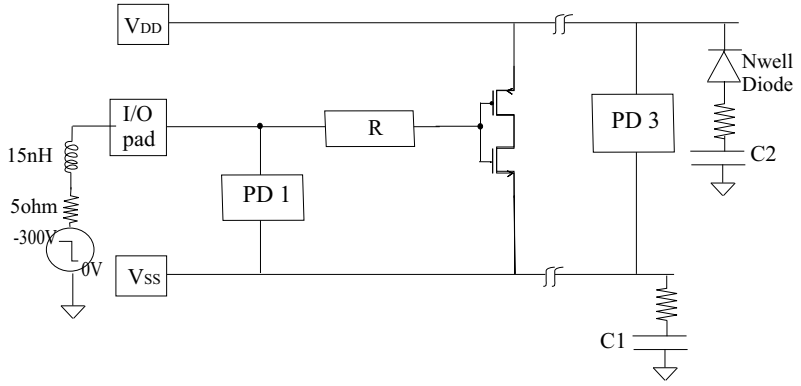


Figure 4.14: Circuit used for simulating CDM stress on the I/O protection design.

Influence of clamping device to Power lines:

In the test structure studied there was no protection device to the V_{DD} line. Hence we wanted to study the effect of having protection devices across the input pad and both the power lines. Figure 4.15 shows the effect of adding a protection device across the input pad and the V_{DD} line on the voltage transients as seen across the gate-oxides of the NMOS and PMOS in the input buffer when the IC is subjected to -300V CDM stress. From the figure 4.15, we see that in the absence of protection device across the V_{DD} line, the voltage drop across the gate-source nodes of the PMOS is much higher than at the NMOS. This is because, the only discharge for the CDM charge coupled with the V_{DD} line is through the power clamp to V_{SS} line into the grounded pin. Note that on including a protection device (ggPMOS), PD2 to the V_{DD} line, we see a large reduction in the voltage transients across the PMOS gate-oxide and the maximum is stress is now at the NMOSt. This is because under negative CDM stress, it is the parasitic diode of the PD2 and the parasitic BJT of PD1 which conducts. On including protection device across each of the power lines to the discharged pin, the CDM stress experience by the gate-oxides at the input buffer is greatly reduced. With protection device at the V_{DD} and V_{SS} power lines, gate-oxides of the NMOS experience higher voltage transients during negative CDM stress and vice versa during positive CDM stress. Hence the more vulnerable location among PMOS and NMOS of the input inverter depends on the amount of CDM current conducted through the V_{DD} and V_{SS} power lines respectively. Assuming the same bus resistance for both the power lines, the larger the current flow, the larger will the potential drop across the

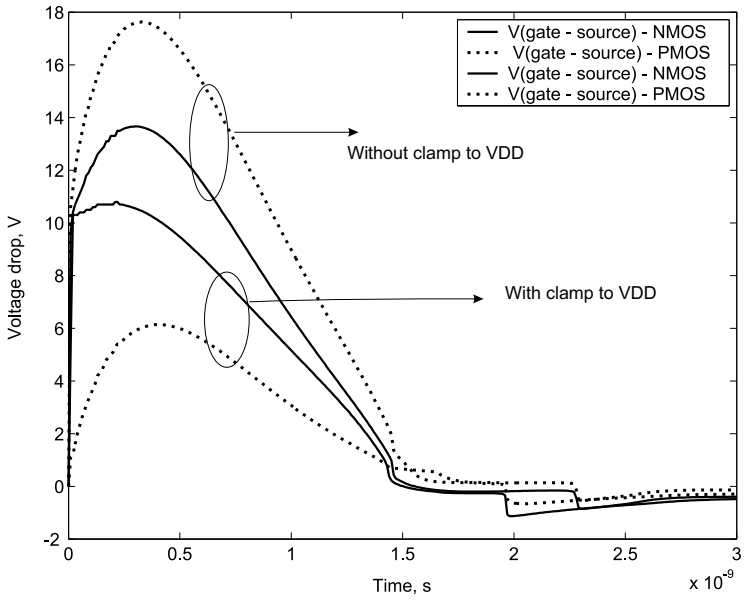


Figure 4.15: Voltage transients across gate-oxides of the MOSts at the input buffer during -300V CDM stress, with and without V_{DD} line clamp.

bus lines be.

Influence of poly resistor:

In section 4.1.1, we have explained the function of a decoupling resistor in the protection design with respect to CDM protection. The circuit used for simulation is shown in figure 4.14. Figure 4.16 shows the voltage transient across the gate-oxide of the NMOSt for different values of poly resistor. From figure 4.16, we see that the voltage transients across the gate-source nodes of the MOSt is independent of the poly resistor used. The expected amount of reduction in the voltage drop as seen by the gate as compared to its pad voltage when the voltage transient applied at the pad is 1V/ps is given in table 4.3. This voltage drop would be seen only in the time period before the protection device turns on. From our simulations we could not see this reduction in the voltage transients seen at the gate. This is because even before the protection device gets turned on fully there is some leakage current flowing through the protection device which reduces the actual voltage transients seen at the input

Table 4.3: Expected voltage drop across the poly for different values of poly resistor.

R [Ω]	C [fF]	RC [ps]	ΔV [V]
10	5	0.05	0.05
100	5	0.5	0.5
1000	5	5	5

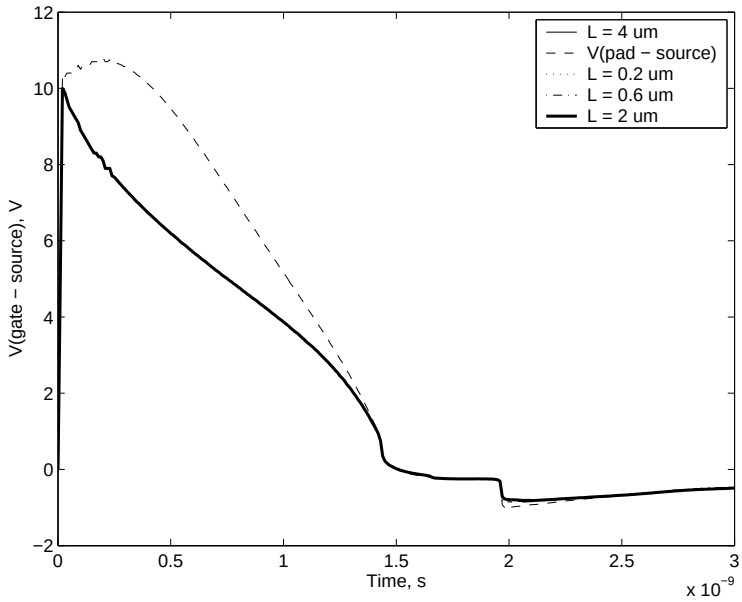


Figure 4.16: Voltage transients across gate-oxides of the MOSts at the input buffer during -300V CDM stress, for different values of decoupling resistor.

pad. Added to this effect, the instantaneous turning on of the protection device (gate-length = 0.6μm) did not give any chance for the poly resistor to play any significant role in reducing the voltage transients as seen by the gate-oxide.

Influence of additional clamp:

Figure 4.17 shows the influence of resistor variation on the voltage transients across the gate-oxide of the NMOSt in the presence of an additional clamping device and the current flowing through the added clamp. The source of the

added clamps PD4 and PD5 is connected to the same power lines as that of the input buffer. Hence the maximum voltage seen across the gate-oxide is determined by the voltage drop across this clamping device. Figure 4.17 shows in

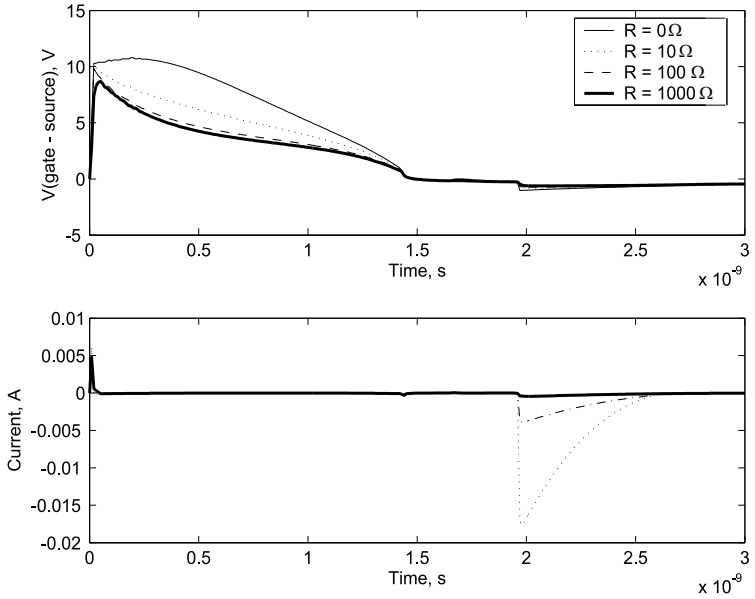


Figure 4.17: Voltage transients across gate-oxides of the MOSts at the input buffer during -300V CDM stress, for different values of decoupling resistor in the presence of an additional clamp and the current flowing through the added clamp.

the presence of the additional clamping device, variation in the poly resistor makes a significant impact on the voltage transients across the gate-oxide. The added clamping device provides a low impedance path for the ESD current. The voltage drop across the resistor, caused by the current flowing through the added clamp is the reduction in the voltage as seen across the gate-oxide as compared to its pad. Unlike in the design with only resistor variation, the influence of resistor is felt throughout the entire pulse, whenever the voltage transient across the added clamp rises above its trigger voltage. Thus the benefit of a poly resistor is maximally utilized in the presence of an additional clamping device close to the gate-oxide to be protected.

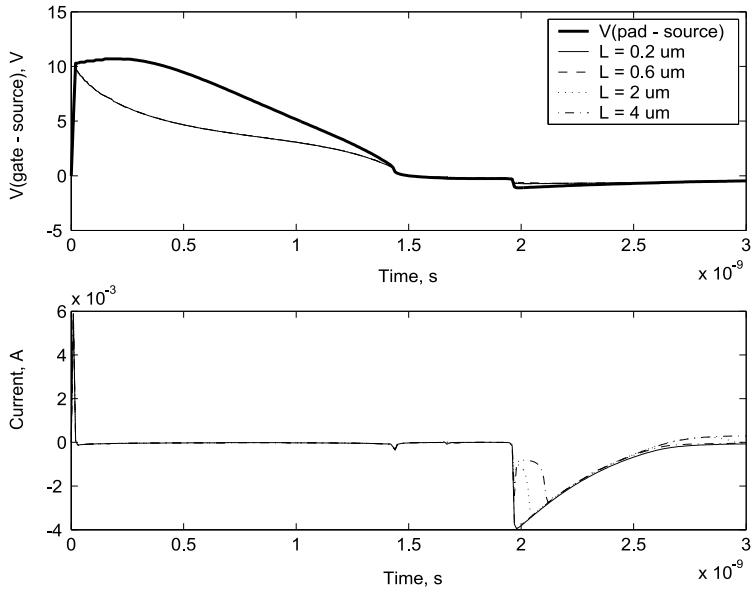


Figure 4.18: Voltage transients across gate-oxides of the MOSts at the input buffer during -300V CDM stress, for different gate-lengths of the added clamp and the current flowing through the added clamp.

Influence of Gate-length of the added clamp:

Figure 4.18, shows the influence of gate-length of the added clamp on the voltage transients seen across the gate-oxide. The shorter the gate-length of the clamp, the shorter would be its turn-on time and hence the quicker is the protection. Once the clamping device begins to conduct, the voltage drop across the poly resistor helps in the turning on of the primary protection. Thus maximum utilization of all the components in the protection design can be made. The benefit of faster turn-on of the added clamp will be seen only when the primary protection does not turn on. From figure 4.18, we do not see any significant reduction in the voltage transients seen by the gate-oxide with reduced gate-length. The added clamp acts as a standby at times of emergency when the voltage drop exceeds its turn-on voltage level and the choice of the gate-length of the clamp does not have any significant impact on the voltage transients.

4.3.2 Output Protection Design

We have shown that CDM stress at an input pad results in the voltage overshoot across the gate-oxides of the MOS transistor in the input buffer, resulting in gate-oxide failure. In the case of a CDM stress on the output pad, the voltage drop overshoot is across the drain and source nodes of the MOS transistors in the output buffer. Thus CDM stress on the output pad can result in the turning on of the MOS resulting in thermal breakdown if the size of the output buffer is small $i.e.$ thermal failure of output buffer depends on its device dimensions. The simulation study done below is useful if the dimensions of the MOS at the output buffer is close to the dimensions of MOS in the internal circuit. The aim of this simulation analysis is to study the influence of various design parameters on the the discharge current flowing through the MOS transistors in the output buffer.

Influence of poly resistor:

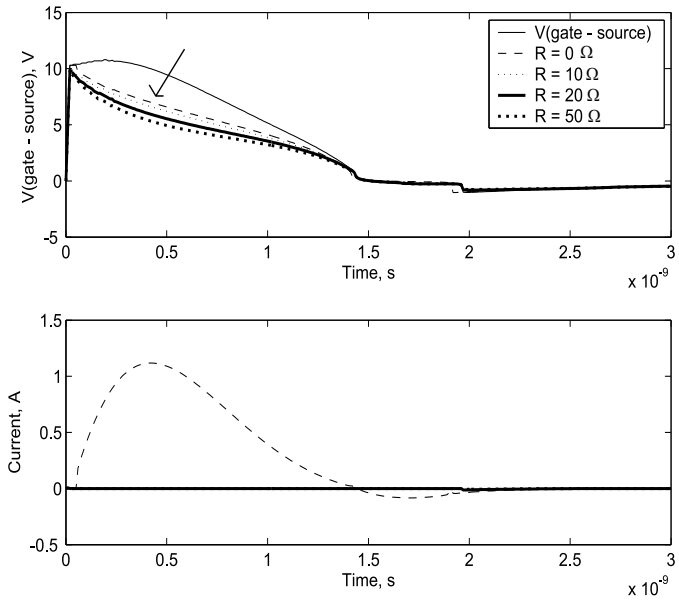


Figure 4.19: Voltage transients across MOSts at the output buffer during -300V CDM stress, for different poly resistor values and the current flowing through the output driver.

The role of the decoupling resistor in the output buffer is to limit the current flowing through the circuit to be protected. Figure 4.19 shows the voltage and current transients across the NMOS of the output buffer when subjected to -300V CDM stress. As the poly resistor is increased, both the voltage transients across the MOS and the current flowing through it decreases.

Influence of gate-length of the MOS:

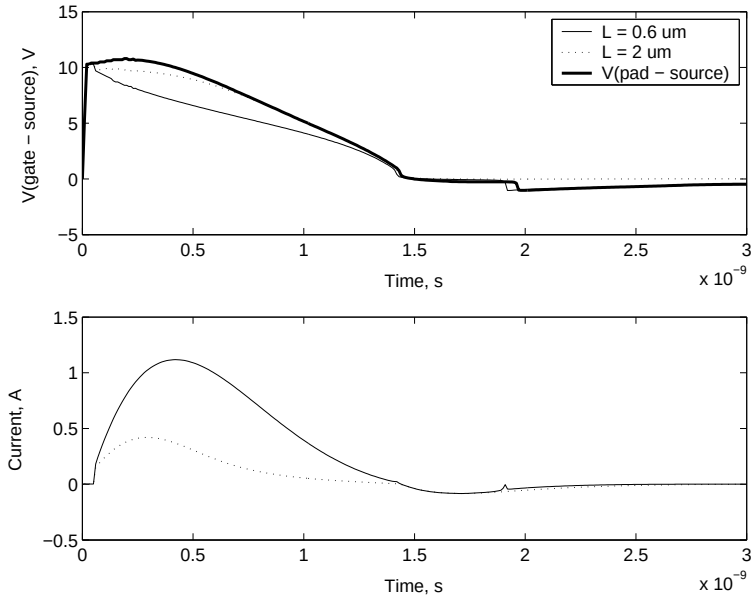


Figure 4.20: Voltage and current transients across the MOSts of different gate-lengths at the output buffer during -300V CDM stress.

Figure 4.20 shows the voltage and current transients across the NMOS of the output buffer for different gate-lengths. From the figure we see that the influence of gate-length is similar to the role of decoupling resistor (See figure 4.19). For longer gate-lengths, the transistor needs more time to turn on and thus has a lower probability of carrying large ESD current. Hence, the longer the gate-lengths of output buffers, the higher is the CDM robustness of the output protection circuit.

4.4 Conclusions

One of the most vulnerable locations to CDM failure is the I/O buffer which forms an interface between the external world and the internal circuitry. Hence ensuring a robust protection design at this interface is a must. Increase of decoupling resistor makes a significant improvement (reduction) in the voltage transients seen across the gate-oxide of the MOS in the input buffer only in the presence of an additional clamping device placed closer to the gate-oxide to be protected. But care should be taken that the current flowing through the added clamp during CDM stress is below the maximum current level which the clamping device can safely handle without thermal breakdown. The gate-length of the added clamping device does not affect the voltage transients seen by the gate-oxide of the input buffer. Regarding output buffers, the CDM stress is across the drain and source of the MOS, which can result in the turning on of MOS and can result in its thermal breakdown if their device dimensions are small. Hence any protection design must aim to reduce the ESD current conducted through the output buffers. Increase of poly resistor and gate-length of the output buffer helps in reducing the current flowing through the MOS transistors in the output buffer.

5 Chapter Package Influence

CDM is often referred to as a package related ESD problem. This stresses the fact that the CDM threshold level of a given circuit design varies with package type. As a result, even if the circuit design remains the same, CDM measurements have to be repeated if they are housed in different packages. In this chapter, a suitable method by which one can extrapolate the CDM threshold level of a circuit design in a given package to other packages is proposed.

5.1 Introduction

In a CDM type of electrostatic discharge, IC is both source of the discharge current and part of the discharge path. The amount of charge delivered to the circuit for a given stress level is greatly determined by its package capacitance[1], while the distribution of the discharge current and hence the failure location in the circuit depends on the circuit design. In other words, the CDM threshold level depends on both the circuit design and the type of package. The package type and the circuit design are completely inter-related and it is impossible to quantify one as CDM robust independent of the other. As a result, even if the circuit design remains the same, CDM measurements have to be repeated if they are housed in different packages.

There are several CDM papers which report on the strong dependency of the failure level to the package type [25, 26, 31, 33, 37]. But until date there is

[1] package capacitance, a collective term for all the capacitors formed by the various conducting layers with the package.

no systematic approach of characterizing the package properties. Tilo Brodbeck [51], had mentioned about the possibility of extrapolating CDM results of a circuit design in one specific package to other packages by means of tabulated peak values of the total discharge currents measured in the different packages. Apart from needing CDM discharge current measurements for each package, this approach is based on the assumption that CDM failure level is only related to voltage overshoots. Whereas in reality we do see thermal failure from non-uniform conduction of CDM current [1, 5].

In this chapter, we present a systematic method of evaluating the influence of the package parasitics on the CDM discharge current based on the equivalent circuit model of CDM stress proposed in chapter 2. From this knowledge a suitable method to extrapolate the CDM threshold level for a given circuit design in different packages is proposed. As this method is based on simulations, it can save a large amount of time consumed in repeating the CDM measurements done on the same circuit design in different packages. The correctness of the proposed method is verified by CDM measurements on identical test structures housed in plastic and ceramic packages.

5.2 Package capacitance - CDM current source

The total current flowing through an IC during CDM stress is from the discharge of various capacitors formed by the different conducting layers in the IC with the package. This is explained in detail in chapter 2. Though the capacitors formed by both the circuit design and package contribute to the total CDM current, the contribution from the circuit design is too small to cause any significant damage to the circuit and hence can be neglected. It is not wrong to assume that the entire CDM current is from the discharge of package capacitance $i.e.$ capacitors formed by the IC package which includes the die attachment plate,C_{SUB} and pin lead frame,C_{PIN} [45].

The type of failure and the failure location is determined by the discharge path of the CDM current through the circuit, which in turn depends on the layout design of the circuit. For a given circuit design, the discharge current distribution will be almost the same for all package type. And what would differ greatly from one package to another is the discharge current delivered to the circuit at a given stress level. Figure 5.1 gives an equivalent circuit representation of an IC under CDM set-up, showing the various package capacitors C_{SUB} and C_{PIN} and their discharge path through the IC die when a particular pin is CDM stressed.

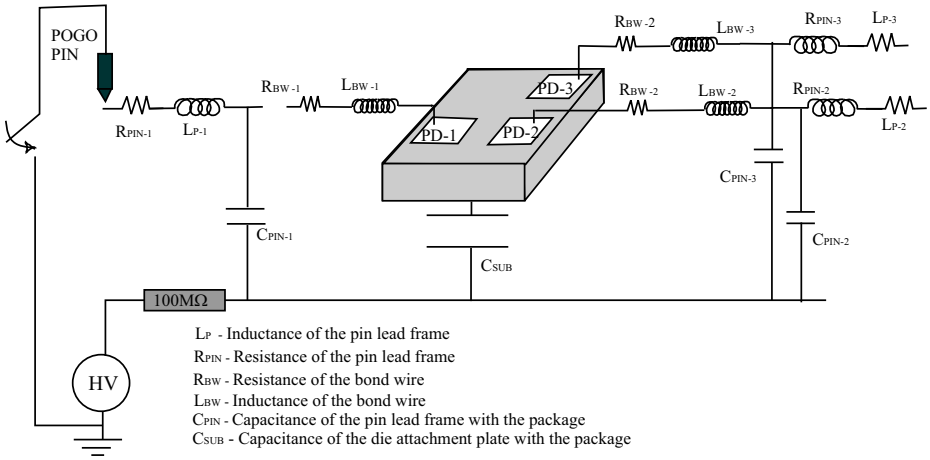


Figure 5.1: Cross-Section of an IC under CDM stress test, showing the various package parasitic elements in the IC.

When a particular pin is discharged, the total current measured is the summation of the discharge currents from all the C_{PIN}'s and C_{SUB}. The discharge current in which we are interested in is the current flowing through the circuit design and not the total discharge current. The contribution of package capacitors C_{PIN}'s and C_{SUB} to this current depends on its magnitude and its discharge path to the grounded pin through the circuit. C_{PIN} is typically much smaller than C_{SUB} and total discharge current flowing through the circuit is mainly from the discharge of C_{SUB}. If we look at the contribution of the individual C_{PIN}'s, we see that the discharge current of the pin under stress flows directly into the grounded pin. Though the magnitude of C_{PIN} can be much lesser than C_{SUB}, in combination with L_{P}, the discharge current of pin capacitor under stress, contributes significantly to the total CDM current measured but not to the current flowing through the circuit. Let us consider a lumped equivalent circuit model of two packages namely CDIL24 and PDIL24. Figure 5.3 shows the total CDM current I_{total}, while figure 5.4 shows the I_{SUB} current flowing through the circuit (replaced by 100Ω) in the two packages. The circuit used to simulate the CDM currents is shown in figure 5.2

From figure 5.3 and figure 5.4 we see that the shape of the total CDM current, I_{total} does not vary much between the two packages, while I_{SUB} shows a notable difference in both I_{peak} and $I_{\text{pulse width}}$ between the two packages. The I_{peak} and $I_{\text{pulse width}}$ value in the ceramic housings are higher than their plastic

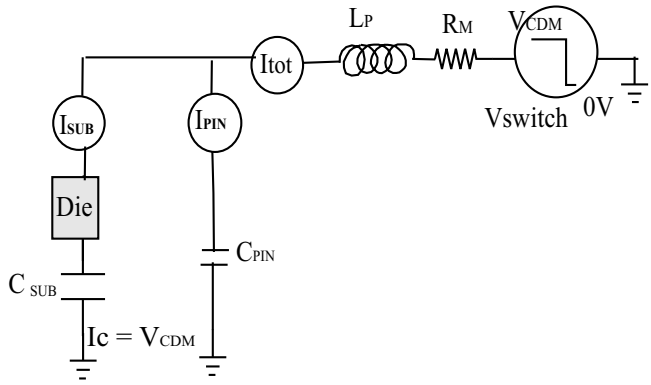


Figure 5.2: CDM circuit used to simulate the discharge current I_{SUB} flowing through the die (represented by 100Ω) in a ceramic and plastic package during CDM stress.

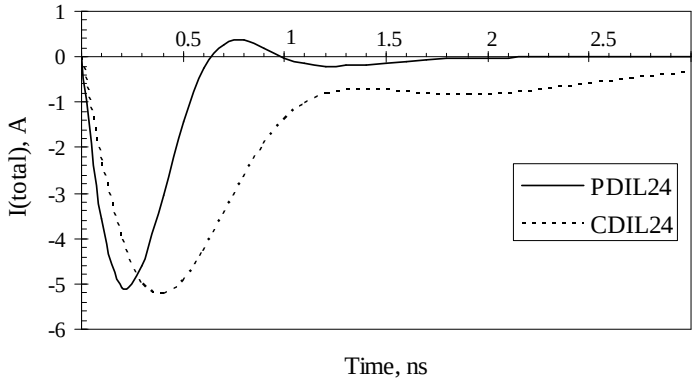


Figure 5.3: Simulated total discharge current,I_{total} in a ceramic and plastic package at $-300V$ CDM stress. Silicon die being represented by 100Ω.

counterparts by a factor of 20% and 30% respectively. We see that though the discharge current of C_{PIN} does not flow through the actual circuit, it contributes to the total discharge current measured. Depending on its relative magnitude with C_{SUB} and its combination with L_{P} it can modulate/influence the shape of the total current measured, misleading our interpretation on the actual discharge current as seen by the circuit. Remember that the previous method of extrapolation shown by Brodbeck [51]was based on the total discharge current measured.

Within a given package, the parasitic elements like pin inductance L_{P}, pin

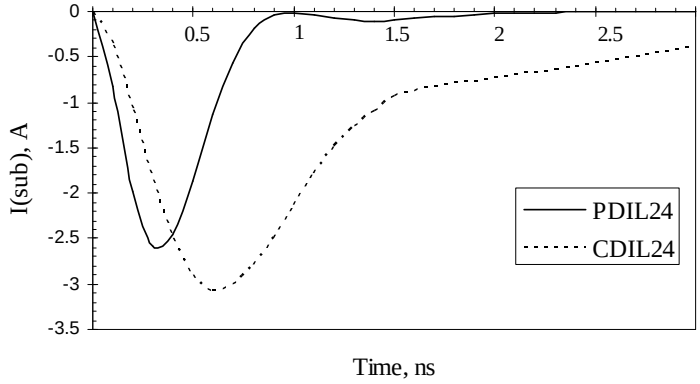


Figure 5.4: Simulated CDM discharge current, I_{SUB} flowing through the die (represented by 100Ω) in a ceramic and plastic package -300V CDM stress.

capacitance C_{PIN} can change from one pin position to another [52]. This has a direct bearing on the shape of the discharge current. Therefore it is necessary to note down the pin positions of the CDM tested IC, to know the exact shape of the discharge current. The contribution from other pin capacitors to the discharge current depends on their type of contact with the substrate and from thereon to the discharged pin. Because C_{PIN}'s are smaller than C_{SUB} and in general as the impedance in their discharge current path to grounded pin is quite large, their contribution to the current flowing through the circuit can be neglected for smaller pin counts. But for higher pin counts, contribution from other pins will be significant and hence cannot be completely neglected.

5.2.1 Correlation of failure level to discharge current

The CDM failure level can be defined as the stress level, beyond which the IC gets damaged. CDM failure on an IC can be from voltage overshoots or from excess current flow through a device.

Failure from voltage overshoot

One typical example of failure from voltage overshoot is gate-oxide breakdown. Gate-oxide breakdown is said to occur if the voltage drop across gate-oxide (gate-source or gate-substrate or gate-drain nodes) of a MOSt during CDM stress exceeds its gate-oxide breakdown voltage. This can happen under

two conditions.

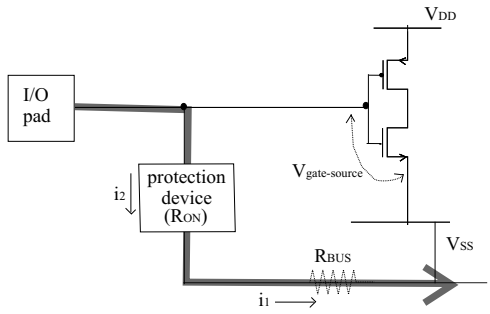


Figure 5.5: Discharge current path through an input protection when the pad is subjected to negative CDM stress.

One, if the turn-on time 't_{on}' of the protection device is longer than the rise time of the CDM discharge current. Two, if the protection devices turn-on in time but the voltage drop along the discharge current path is significant enough to cause the potential drop seen across a gate-oxide to exceed its breakdown voltage. For example, voltage drop across the gate-oxide of an input buffer is given by,

$$V_{\text{gate-source}} = i_1.R_{\text{BUS}} + i_2.R_{\text{ON}} \tag{5.1}$$

where, R_{ON} - On-resistance of the protection device (See figure 5.5),
From equation 5.1, we see that the voltage drop across the gate-oxide depends on the amplitude of the discharge current flowing through it. Thus in context to gate-oxide failure, CDM threshold level is defined as the stress level at which the amplitude of the discharge current through the circuit exceeds a particular peak value. This peak value of discharge current decides the maximum voltage drop across the gate-oxide and hence on the gate-oxide failure level.

Failure from excess current

Excess current flow results in thermal breakdown, as silicon melts from excess heat dissipation. Though the amplitude of the CDM current is quite large, its pulse width or stress time is much shorter than other type of ESD events. The power dissipated from CDM stress does not have enough time to reach the entire volume of the protection device as in the case of HBM or TLP stress. But if the protection device shows slight non-uniform conduction, current conduction gets restricted to a smaller volume of the protection device resulting in

thermal breakdown. Thermal breakdown during CDM stress results from non-uniform triggering of the protection device [1, 29]. Power dissipated during CDM stress after the protection device is turns on is given by joule's law as,

$$\mathbf{P} = \int i_{\text{CDM}}^2 . R_{\text{ON}} dt \tag{5.2}$$

$$= \int i_{\text{CDM}} . V_{\text{hold}} dt \tag{5.3}$$

where, V_{hold} is voltage drop across the protection device. For an ideal protection device, the voltage drop across it is constant throughout the entire period of CDM stress. Hence,

$$\begin{aligned} \mathbf{P} &= V_{\text{hold}} . \int i_{\text{CDM}} dt \\ &= V_{\text{hold}} . Q_{\text{CDM}} \end{aligned}$$

where, Q_{CDM} - total CDM charge stored in the IC.
Thus from equation 5.2, we see that the amount of heat dissipated is directly related to the area under the curve of a CDM discharge current. Thus in context to thermal breakdown, CDM threshold level is defined as the stress level at which the area under the discharge current through the circuit exceeds a particular value. This value of the discharge current decides the maximum heat dissipation needed for a thermal breakdown. Voltage overshoots across the source and drain nodes of MOSts in the internal circuitry during CDM stress can cause unwanted turning on of the internal MOSt devices and may result in thermal breakdown. In other words, thermal breakdown of MOSts in the internal circuitry results from voltage overshoots which is related to the peak value of the discharge current. Thus if the thermal breakdown location is at the protection device then the threshold level of the corresponding circuit design relates to the area under the discharge current flowing through the circuit. But if the failure location is at internal circuitry then the threshold level of the circuit design will also depend on the peak value of the discharge current.

Thus the actual CDM threshold level of a device is in several ways related to the waveform of the discharge current that flows through the circuit. If we can measure or simulate the discharge current flowing through the circuit for a given stress level in different packages, then we can extrapolate the CDM threshold level of a given circuit design in one package to other packages provided we also know the type of failure encountered in it.

5.3 Proposed Package Calibration Method

Because of the large package dependency on the measured CDM threshold level of a given circuit design, it becomes mandatory to repeat the CDM measurements for different packages even if the the circuit design remains the same, thus costing large amount of time. In this section, we present a method by which CDM measurement results of any circuit design in one package can be extrapolated to other packages. As this method is based on simulations, it can save a large amount of time consumed in repeating the CDM measurements for different packages. This method is based on the assumption that the circuit design encounters the same type of failure in all the packages. Also it models the amount of discharge current flowing through the circuit unlike the measured CDM discharge current which gives the total current flowing through the IC.

Let us consider a particular circuit to be housed in package-A (P-A) and package-B (P-B). Let V_{fail}(P-A) be its CDM threshold level on P-A. Then the circuit design's failure level V_{fail}(P-B) in package-B can be extrapolated as follows.

- Perform failure analysis of IC in P-A to know the type of failure.
- Measure the package parasitics of P-A and P-B as explained in annexure 5.4.
- Substitute the corresponding values in the circuit model shown in figure 5.2. Replace the circuit design by any simple component say 100Ω resistor. The circuit design can be replaced by any type of component. The results will not change as long as the same component is used to model the circuit design in both P-A and P-B. Simulate I_{SUB} for CDM stress level at V_{fail}(A) and note the corresponding peak current value I_{peak}(A) of I_{SUB}
- Repeat simulation for different stress level in P-B until I_{peak}(B) equals I_{peak}(A), if failure analysis in P-A had shown failure from voltage overshoot. The corresponding stress level gives the threshold level of the circuit in P-B.
- Repeat simulation for different stress level in P-B until area under the discharge current of I_{SUB}(B) equals I_{SUB}(A), if failure analysis had shown a thermal breakdown.

5.3.1 Validation of the Proposed Method

Two different test structures were housed in both ceramic and plastic DIL24 pin package. One test structure consisted of individual ggNMOSt with different layout parameters in the $0.18\mu m$ technology and the other I/O cells with different design variations in $0.65\mu m$ technology node. In this section, we have applied the proposed method to estimate the failure level of the test structures in the plastic package. But we did not have accurate measurements of the package parasitics. For ceramic packages, we could measure C_{PIN} and C_{SUB} as explained in the annexure. But for the plastic we did not have empty packages to do our C_{PIN} measurements. Hence the values of C_{PIN} for PDIL24, are from the simulated RLC parameters of the package. L_{P} was also taken from the standard RLC package characterization charts for both the packages. Note that L_{P} is the total inductance of the bond wire and the pin lead frame and hence we did not separate L_{P} from L_{BW}. The equivalent circuit model used for our simulations is as shown in figure 5.2. For more accurate predictions of CDM failure level in other packages, intense characterization of package parasitics that affect the CDM discharge current is needed.

Step 1: The package parasitics of both plastic and ceramic packages is enlisted in table 5.1. These values are measured as explained in annexure 5.4.

Table 5.1: Package parasitic values of 24 pin Ceramic and Plastic Dual In Line package.

	PDIL24 C_{SUB}, 4[pF]		CDIL24 C_{SUB}, 14[pF]	
Pin position	C_{PIN}[pF]	$L_{\text{P}}[nH]$	C_{PIN}[pF]	L_{P}[nH]
2	1.6	4.8	2.5	10
6	0.8	1.7	1.4	6
8	0.83	2	2.1	7
9	1.04	2.4	2.5	8.5

Step 2: The values of the package parameters for pin number 2 as marked in table 5.1 are substituted in the circuit model as shown in figure 5.2. The circuit is replaced by 100Ω resistor and I_{SUB} is simulated for different stress levels. The important parameters of the discharge current, namely I_{peak} and the area under the discharge current curve for different stress levels for both CDIL24 and PDIL24 are tabulated in table 5.2. As the value of C_{PIN} and L_{P} changes from one position to another, a table similar to table 5.2 has to be made for each pin position.

Table 5.2: Simulated Discharge current parameters for different stress levels in CDIL24 and PDIL24 housings for pin position 2.

	PDIL24		CDIL24	
Stress Level [V]	I_{peak}[A]	Q_{CDM}[nC]	I_{peak}[A]	Q_{CDM}[nC]
-250	2.2	1.0	2.8	2.0
-300	2.8	1.2	3.5	2.4
-400	3.5	1.6	4.5	3.2
-500	4.5	2.0	5.5	4.0
-600	5.2	2.4	6.8	5.0
-800	7.0	3.2	9.0	**6.2**
-1000	8.8	4.0	11.2	8.0
-1200	10.6	4.8	13.5	9.5
-1500	13.2	**6.0**	17	12.0

Test structures with individual ggNMOSt

Identical test structures of individual ggNMOSt housed in both CDIL24 and PDIL24 were subjected to CDM stress measurements. The test results showed that some devices that had failed around $800V$ in a CDIL24 package failed only around $1500V$ or higher stress levels in PDIL24 plastic housings. Failure Analysis of these test structures showed thermal failure due to non-uniform triggering of the protection devices. In this case failure was from excess heat dissipation under CDM Stress. Hence the area under the curve or the charge delivered through the protection device should be computed to compare its failure level in different packages. Table 5.3 gives the simulated and measured threshold level for few ggNMOSts in the plastic package. From the table, it is seen that the predicted and measured failure levels coincide quite well.

Table 5.3: Simulated and Measured CDM threshold level in PDIL24 package for several ggNMOSt devices.

	CDIL24		PDIL24	
	measured		simulated	measured
Device	V_{fail} [V]	Q_{CDM}[nC]	V_{fail}[V]	V_{fail}[V]
1	-800	6.5	-1500	-1500
2	-1000	7.5	-1800	-1700
3	-400	4.5	-1000	-1500
4	-700	8.0	-2000	-2200
5	-700	9.0	-2400	above -2500

Test structures with I/O cells

CDM measurements on the test structures with I/O cells of different design variations in 0.65μm technology node were made in both CDIL24 and PDIL24 packages. The input cell circuit design is shown in figure 5.6. CDM withstand level of input cells for varying values of poly-resistor is plotted in figure 5.7 for both PDIL24 and CDIL24 packages. From figure 5.7 we see that the CDM threshold level is independent of the poly-resistor value.

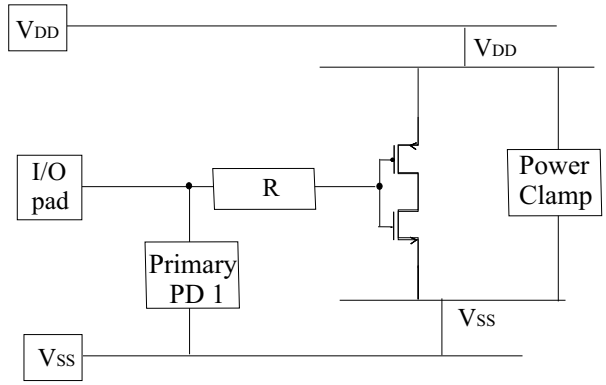


Figure 5.6: An Input cell of the test structure.

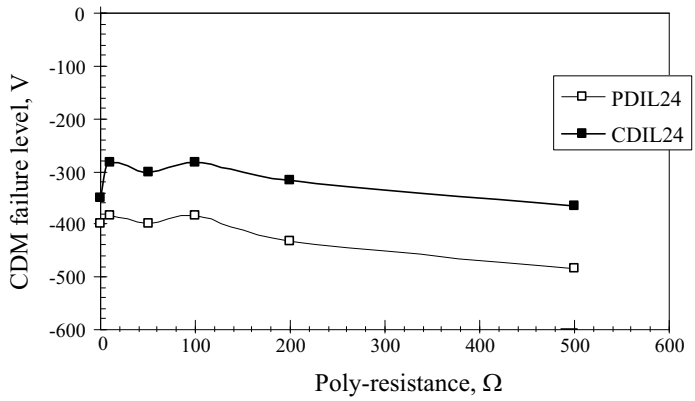


Figure 5.7: Influence of poly resistance on the CDM failure level of the input buffers in plastic and ceramic package.

This observation remains the same for both ceramic and plastic packages, but the level of failure is different for the two. FA study on these samples showed gate-oxide failure at the PMOSt in the input buffer. Hence I_{peak} is taken as the failure criteria to estimate its failure level in plastic packages. Table 5.4 gives the simulated and measured threshold level for different input cells with various poly-resistor values in the plastic package.

Table 5.4: Simulated and Measured CDM threshold level in CDIL24 package for input cells with varying poly-resistor values

Device	PDIL24		CDIL24	
	measured		simulated	measured
	V_{fail} [V]	I_{peak}[V]	V_{fail}[V]	V_{fail}[V]
1	-385	3.6	-340	-285
2	-400	3.7	-350	-300
3	-385	3.3	-300	-315
4	-415	3.7	-340	-320
5	-500	4.5	-420	-385

5.4 Conclusions

A practical method by which CDM threshold level of a given circuit in one package can be extrapolated to other packages has been proposed. The discharge current flowing through the circuit determines the failure level of a given circuit. I_{peak} of I_{SUB}, the current flowing through the circuit determines the voltage drop across a device and the area under I_{SUB} directly relates to the amount of heat dissipation. Hence for effective extrapolation of CDM results, prior knowledge on the type of failure is a must. I_{total} measured can be quite different from the actual current flowing through the circuit because of the direct discharge C_{PIN} to the grounded pin. The simulation method proposed helps in modelling the actual current that flows through the circuit and thus provides better accuracy. The proposed method has been verified by CDM measurements done on identical test structures in different packages.

Appendix

Measurement of Package parasitics
The various package parameters and their method of measuring these parame-

ters are explained in detail in this section.

1) Pin Inductance L_P: L_P represents the inductance of the lead frame of the pin and its bond wire. To measure this parameter, dummy packages are made with bond-wires of approximate length attached from each pin to the paddle or silicon die without any circuit design, from each lead as shown in figure 5.8. Two leads having similar geometric properties are selected and S parameter

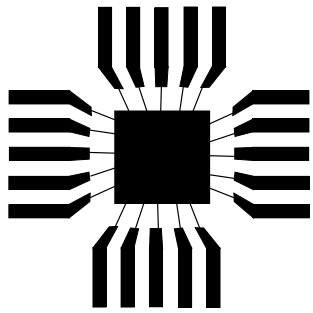


Figure 5.8: Package sample for resistance and inductance measurements. Lead frames are shorted to paddle or test die.

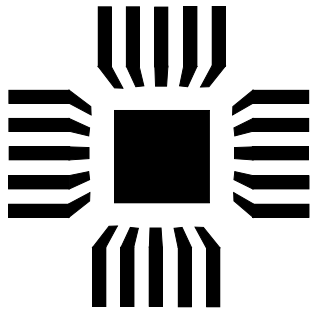


Figure 5.9: Package sample for capacitance measurements.

measurements are done to calculate the inductance of entire loop. The value is divided by two to give L_P. These measurements are carried out by mounting the IC on special boards designed with topside ground and isolation pads for the leads under test. This is to eliminate the mutual inductance element from the measurement. Inductance measurement always includes the inductance of the bond wire. An inductance of 2nH is added to the pin inductance obtained from the package to account for the inductance from the test set-up, while

simulating CDM discharge event.

2) Pin Capacitance $C_{\mathbf{PIN}}$: C_{PIN} is the self capacitance of the lead under test with the field plate/package. To measure this capacitance the bond wire connections to the silicon or IC are removed as shown in figure 5.9. The sample is positioned on a test fixture that has a topside ground plane. The lead under test is isolated and all other package leads are connected to a common potential (same as the test fixture) and the impedance measurements are carried out to measure C_{PIN}.

3) Pin Resistance $R_{\mathbf{P}}$: R_{P} represents the total resistance of the lead frame of the pin R_{PIN} and bond wire P_{BW} connecting it to the die. This parameter is measured from DC current measurements on two identical pins in the test sample as shown in figure 5.8. The resistance offered from the test set-up is also added to this value while simulating the CDM discharge event.

4) Substrate Capacitance $C_{\mathbf{SUB}}$: Substrate capacitance represents the capacitance of the die attachment plate with respect to the field plate/package. The value of this capacitance is much larger than any of the pin capacitances. This is measured either by shorting one of the lead pins to the die attachment plate and capacitance of this pin lead would then give C_{SUB} or by drilling a hole from the backside until contact to the die attachment plate is established. The capacitance between the package and the die attachment plate is then directly measured to give C_{SUB}.

Alternately, all these parameters can also be calculated if the dimensions of the package and the properties of the lead frame and package are known precisely.

6 Chapter Substrate Influence

In this chapter, the potential CDM current sources that discharge during a CDM-ESD event are studied. The importance of substrate capacitance and the possible CDM failure due to direct gate-substrate voltage overshoots are investigated in great depth. For the first time, a suitable method of modelling this capacitance and its discharge path through the circuit in the third dimension, namely the substrate is presented. The limitations of the circuit model and the impact of grid size on the accuracy of the simulation results is discussed. Lastly, a general stepwise sequence by which one can build a full chip circuit model to study the CDM performance of any given IC is presented.

6.1 Introduction

A charged IC is equivalent to several pre-charged capacitors. Grounding of an IC pin initiates the discharge of all these capacitors resulting in voltage transients along their discharge paths. Such voltage transients can result in gate-oxide failures if the potential drop seen across the gate-oxide exceeds its breakdown voltage. Hence the golden rule for CDM protection is: "Avoid voltage overshoot across the gate-oxides in a circuit above their breakdown voltage" [12]. But to avoid the voltage drop, one should know the likely gate-oxides (locations) on the circuit which can be prone to large voltage drops during CDM stress. To find the CDM sensitive locations (locations prone to large voltage overshoots), we need to model the source of charge and its path through the circuit.

The previous chip level CDM charge transfer model presented by Lee [24]

is incomplete as it models only the discharge of bus line capacitors namely C_{SS} and C_{DD}, their distributed current path through the circuit and the consequences of the potential drop across the bus lines on the voltage transients across the gate-source nodes of MOSts. In short it models the CDM current sources formed by the circuit layout and studies the result of voltage transients across the circuit elements during CDM discharge. For large ICs where there is much power routing around and over the chip, C_{SS} and C_{DD} can have a significant contribution to the total discharge current. But nevertheless the underlying die attachment plate on which the silicon chip is mounted also forms a large capacitance (we refer to this capacitance as C_{SUB}) with the package and its effect on the total CDM discharge current should not be neglected. The influence of the discharge of C_{SUB} on the CDM performance of a circuit has not been investigated. The discharge of C_{SUB} not only causes voltage transients across the circuit elements but also between the circuit elements and the underlying substrate. Such voltage overshoots can also result in gate-oxide failure of MOS. Although the importance of including direct discharge path through the substrate has been emphasized lately [50], no one has so far explored the effect of C_{SUB} discharge on the CDM performance of a circuit in a full chip level.

In this chapter, we have focussed our attention to understand the role of C_{SUB} on CDM performance of an IC by trying to answer the following questions. What is the contribution of the C_{SUB} discharge current as compared to other IC capacitors that discharge during CDM stress? What are the discharge paths available for C_{SUB}? How can one model the voltage transients set across the substrate during CDM stress? And what are the circuit layout designs that needs to be modified to overcome the danger of substrate-gate voltage overshoot.

6.2 Significance of C_{SUB}

6.2.1 C_{SUB}, Major CDM current source

In Chapter 2, it has been shown that CDM discharge current is the summation of all the discharge currents of the various capacitors formed by the conducting layers in an IC with its package. The influence of these capacitors on the CDM performance of a circuit design depends on its magnitude and its discharge path through the IC circuit. Among the various capacitors formed by the circuit design with the package, the capacitors formed by the V_{DD} and V_{SS} lines

Table 6.1: Calculated and Measured values of important IC capacitors. The superscript *d, nd* stands for discharged and non-discharged pins respectively.

CDM current sources	CDIL24 [pF]	PDIL24 [pF]	Discharge current path
C_{SS}	0.1	0.1	bus line + PD^{d}
C_{DD}	0.1	0.1	bus line + PD^{d}
C^{d}_{PIN}	1 - 3.5	0.5 - 2	PDnd + bus line + PD^{d}
C^{nd}_{PIN}	1 - 3.5	0.5 - 2	discharge pin
C_{SUB}	14	4	substrate + circuit elements + PD^{d}/discharge pin

namely, C_{DD} and C_{SS} respectively have the largest magnitude. The magnitude of C_{DD} and C_{SS} depends on the circuit design. But apart from them, there are conducting metal layers like the die attachment plate and pin lead frame in the IC housing/package which are also capacitively coupled to the charge in the IC package. Table 6.1 gives the magnitude of few of the major CDM current sources and their discharge path to the grounded pin for an IC in a CDIL24 and PDIL24 pin package. The values of C_{DD} and C_{SS} are calculated assuming the V_{DD} and V_{SS} metal layer to extend all over entire IC chip and the chip size to be 1mm·1mm. C_{PIN} and C_{SUB} are obtained from package parasitic measurements as explained in chapter 5. From these values, we clearly see that C_{SUB} has a significant contribution to the CDM current. The contribution of C_{SUB} and will depend on the type of package used and the pin counts. In general for all the packages the contribution to the discharge current from C_{SUB} will be quite significant and hence should not be neglected. How do these values affect the potential transients in a circuit during CDM stress? The larger the capacitor, the larger is the discharge current and hence the larger is the potential drop across its discharge current path. Thus we see that C_{SUB} has a prominent role to play in affecting the voltage transients across the circuit not only because of its large magnitude but also because of its discharge current paths to and through the circuit.

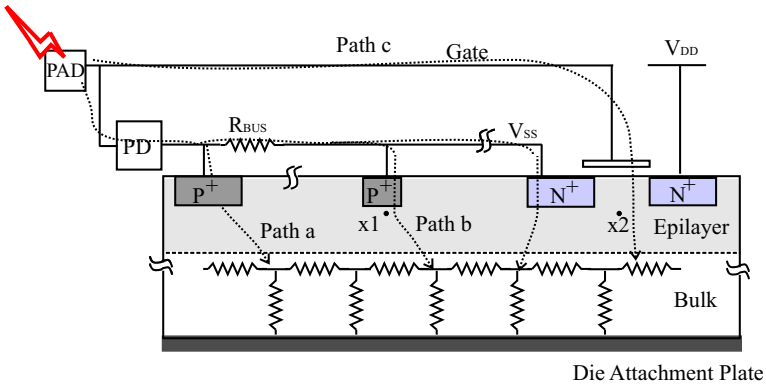


Figure 6.1: Cross-section of an IC showing the various possible discharge paths for the discharge current of C_{SUB}.

6.2.2 Distributed discharge current path of C_{SUB}

C_{SUB} is a resistive capacitor in the sense that the path of discharge current from the die attachment plate to the ground is through the substrate (bulk material) into the grounded pin. All the circuit elements in a given circuit design has either resistive or capacitive connection to the substrate and thus to C_{SUB}. These different connections on the substrate provide innumerable number of discharge paths for C_{SUB} to the grounded pad (See figure 6.1). This also explains the distributed nature of CDM failure and its sensitiveness to the substrate resistivity [9, 52]. The different discharge paths available can be classified into three types,

Type-a: Direct P^+ substrate contacts shown by path-a in figure 6.1. This is the lowest impedance discharge path for C_{SUB}. The P^+ substrate contacts are shorted to the V_{SS} power rails at certain locations. This makes the power rails also one of the most desired discharge path for the designers.

Type-b: Parasitic diodecontact with the Nwell regions shown by path-b in figure 6.1. This path provides a low impedance path only during one polarity.

Type-c: Capacitive current through the gate and field-oxide capacitors. CDM current can be considered as a transient signal and thereby the

capacitors can also provide discharge current paths for C_{SUB} capacitor. An example of this type is shown by path-c in figure 6.1

The majority of the discharge current from C_{SUB} would flow through P^+ substrate contact to the V_{SS} rail and in the suitable polarity also through the second parasitic path to the V_{DD} lines. This is because, apart from being low impedance paths, the power rails are also connected to all the I/O pads (grounded pins) via one or more protection devices. Depending on the amount of discharge current flowing through the power lines and the bus line resistance involved in the discharge current path, the potential seen across the gate and source nodes can exceed the breakdown voltage resulting in gate-oxide damage. But we are not studying this effect. Instead our question is **"Assuming a zero bus line resistance, do we still foresee any danger of CDM failure?"**

The discharge current flow does not only cause voltage transients across the circuit elements but also voltage transients across the substrate (See figure 6.1). Potential at any substrate node will depend on the type of substrate contact it makes with the circuit element, the type of contact this circuit element makes with the discharged pin and its distance from the nearest P^+ contact. Let us look at the likely potential drop across a MOSt gate with respect to its substrate during a CDM stress. Let $x1$ be a substrate location below a P^+ substrate contact and $x2$ the substrate node below a MOSt. The potential drop across the gate and substrate node during CDM discharge is given by,

$$\begin{aligned} V_{\text{gate-substrate}} &= V_{\text{x1}} + V_{\text{x1x2}} \\ &= V_{\text{gate-source}} + i.R_{\text{x1x2}} \end{aligned} \tag{6.1}$$

where,
R_{x1x2} - Effective substrate resistance between x1 and x2,
i - Effective discharge current flowing from x1 to x2.

From equation 6.1 we can foresee a **potential danger of gate-oxide failure arising from the excess potential drop seen by the substrate node as compared to its source from the discharge current of C_{SUB} flowing through the substrate.** Having analyzed the significant role of C_{SUB}, we proceed further to model this capacitor to study the voltage distribution in greater detail and investigate the various possible methods of reducing voltage overshoot of substrate node as compared to its source.

6.3 Circuit model for substrate

Circuit layout designs are 2-D in nature. They do not take into account the underlying substrate which is common for all the elements in the circuit. To model an IC under CDM event, especially when you want to study the discharge path of C_{SUB}, one needs to take into account this third dimension as well.

6.3.1 Existing substrate models

With the trend towards increasing complexity of circuit designs and ever increasing demand for higher operating speeds, the parasitic effects of the substrate on the circuit performance have become unavoidable [53, 54]. For example, a well known problem encountered by ICs operating at very high frequency is the parasitic substrate noise coupling generally known as on-chip cross-talk. In mixed signal ICs, signals from the digital block can be picked up by the substrate in the analog block and affect the circuit performance, despite the presence of isolation trenches used in the layout design [55]. It has therefore become mandatory to include the influence of substrate in the circuit models used to evaluate the circuit performance of a given design. Most of the research in this field of substrate modelling is generally limited to the epilayer of the IC die. The requirements of a substrate model to study CDM behavior of an IC varies from those of the conventional substrate models. The former deals with modelling the signal propagation from the die to a point on the circuit through the substrate, while the latter deals with modelling the parasitic coupling of a signal from one point on the circuit to another via the substrate [56].

6.3.2 Substrate model applicable for CDM event

A major amount of CDM charge flows from the die pad capacitance C_{SUB} via the substrate to the discharged pin. It was shown in section 6.2.2 that the discharge path of C_{SUB} is not only the P+ substrate contacts but also several other parasitic paths like the pn junction diodes formed by the Nwell, gate-oxide capacitors and so on. When an IC is subjected to CDM stress, C_{SUB} will discharge through any available low impedance path, creating a voltage gradient across the substrate. The magnitude of this voltage gradient depends on the substrate resistivity. The higher the substrate resistivity, the higher is the gradient. The voltage drop across the gate-substrate nodes may result in

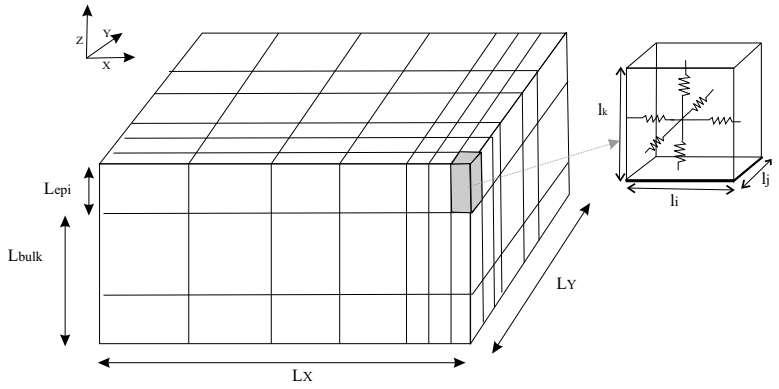


Figure 6.2: Lumped resistive model for a unit volume of silicon substrate.

gate-oxide failure. To study the voltage transients across the substrate, a 3-D circuit model of the substrate is needed. A simple method of realizing a 3-D equivalent circuit model for the substrate is detailed in this section.

The entire volume of silicon die is subdivided into smaller unit volumes of parallelepipeds as shown in figure 6.2. Each subunit volume has at least two layers (subunits) to include the epilayer and the bulk. The epilayer and the bulk can have different doping densities and hence different specific resistances. Each unit volume element is approximated by two lumped resistors in each of the three coordinate directions as shown in figure 6.2. The equivalent value of the resistance in the X, Y and Z directions in each subunit is given by,

$$R_{\mathrm{i}} = \frac{\rho l_{\mathrm{i}}}{l_{\mathrm{j}} l_{\mathrm{k}}} \tag{6.2}$$

where, ρ- substrate resistivity of the bulk/epilayer
$l_{\mathrm{i}}, l_{\mathrm{j}}, l_{\mathrm{k}}$ - dimensions of the subunit in the x, y and z direction respectively.

The capacitance attached to each unit volume is given by,

$$C_{\mathrm{S}} = \frac{C_{\mathrm{SUB}} l_{\mathrm{i}} l_{\mathrm{j}}}{L_{\mathrm{X}} L_{\mathrm{Y}}} \tag{6.3}$$

This capacitor is attached only to the bottom most subunit which connects to the die attachment plate as shown in figure 6.2. One end of this resistive network in Z direction is connected to the substrate capacitance and other end to the circuit elements in that volume. By placing many such parallelepiped

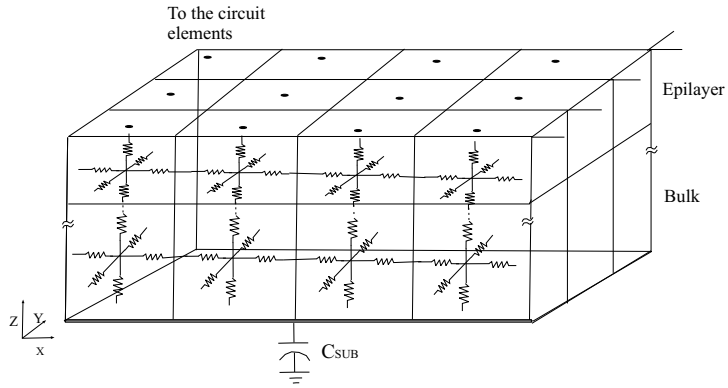


Figure 6.3: A portion of the 3-D resistive network used to model the substrate.

(or resistive cells) side by side, the entire silicon substrate of the IC chip can be reconstructed by a 3-D resistive network as shown in figure 6.3.

6.3.3 Circuit model for MOS

Any circuit element makes either direct resistive or indirect capacitive contact with the underlying substrate. Under CDM condition, a static logic inverter can be modelled as shown in figure 6.4. This model is valid under the assumption that the chip is not powered up and it is only the parasitic contacts that provide the discharge current path from the substrate to the grounded pin or bus lines. The protection devices are replaced by their compact circuit models which can model the high current transient behavior of the protection devices. A detailed description of the protection device behavior under CDM stress is given in chapter 3.

6.3.4 Simplifications on the model

In a device or circuit simulation, we model the behavior of a continuous system by few discrete elements. In this process we use certain simplifications few of which are listed below.

1. The lumped resistor model representation of a unit volume element assumes that the potential is constant over each of the volume element's faces and that the current is uniform in any coordinate direction between

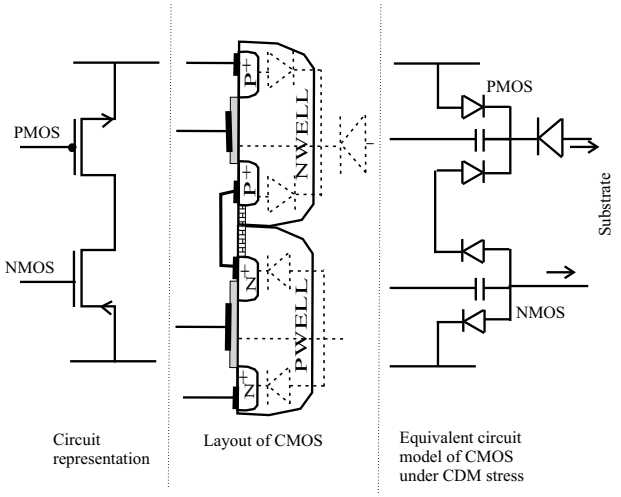


Figure 6.4: Layout of a logic inverter showing its parasitic contact with the substrate and its equivalent circuit model under CDM stress.

the two parallel faces. Hence for high resolution, one should have minimum grid spacing everywhere in which case the number of circuit components would be enormously large for the simulator to handle. Therefore we need to vary the grid size with minimum spacing at locations which require maximum resolution and larger spacing elsewhere. As the aim of the simulation is to identify the vulnerability of a location to voltage overshoot, those locations subjected to maximum potential gradient during a given CDM stress is provided with minimum grid spacing. This limitation on the model can be compensated by proper choice of grid size.

2. In a realistic situation, the protection elements and circuit elements get heated up during an ESD event because of the large current flowing through it. Heating results in increase of R_{ON} resistance and thus affects the current and voltage transients. But in our circuit model, we have not taken into account the variation in resistance from heating during CDM stress. This simplification can be justified as the heating effects of the CDM discharge current is not very significant because of the very short duration of the CDM stress.

3. Strictly speaking each node of the substrate is also coupled to the charge in the package as it is a semiconducting material. But this effect is not

captured in the model. The cost we pay would be the decrease in the amount of discharge current we see from the simulation.

4. The interface of a highly and lowly doped material shows slight non-linear diode like behavior and not an ohmic connection as captured in our model.

6.3.5 Simulation Difficulties

The circuit model presented can be considered as an attempt to achieve device simulation on a large scale (entire chip including the entire circuit design). The presence of large resistive networks and unstable protection devices along with the large voltage transients result in the following simulation difficulties.

1. **Large Computational time:** The time taken for the simulation to complete depends on the number of nodes (equations to solve$\approx$ 60,000) in the circuit and the time taken for the solutions to converge. The large resistive network used for simulating the substrate, increases the number of nodes and hence the equations to be solved. The simulation time is approximately 15 hours when run through a pentium three desktop.

2. **Convergence Difficulties:** Protection devices which show snapback behavior are very unstable in terms of simulation. The snapback behavior of these devices results in sudden a drop of potential across the device resulting in convergence difficulties. This places a limitation on the maximum time step required for convergence. Presence of very large resistance in the order of MΩ modelling the substrate resistance in series with a small resistor in the order of mΩ modelling the bus line resistance also makes it difficult for the simulator to choose the proper time step.

3. **Extremely Fast transients:** A CDM discharge is an extremely fast transient ESD pulse. This is modelled by the sudden large voltage transient of V_{SWITCH}. Although this is the realistic case, such a sudden change from few hundreds of volt to 0V within one time step ($\approx$ 100fs), results in convergence difficulties.

6.4 The distribution of substrate contacts

Consider a silicon die of area 1000μm$\cdot$1000μm area subdivided into smaller unit areas of 100μm$\cdot$100μm. Each unit volume is modelled as a resistive net-

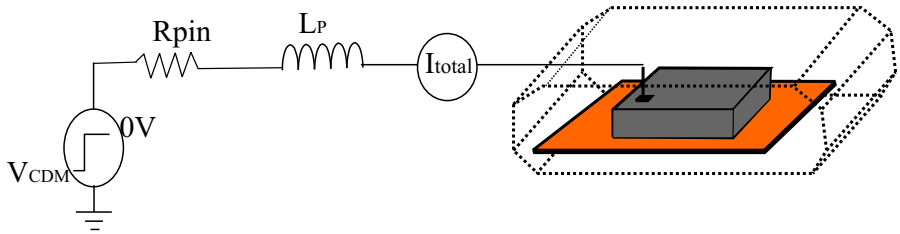


Figure 6.5: Overview of Silicon die with one single substrate contact subjected to CDM stress.

work as explained in section 6.3.2. The resistive network ends up in a node to which the circuit elements are connected to, as shown in figure 6.3. The potential drop across all these nodes on the silicon die with respect to a grounded location is studied. In the following exercise, we study the potential drop distribution for three types of substrate:

High-ohm High ohmic substrate, where the bulk and the epilayer have the same doping and hence the same resistivity (10^{15}cm^{-3}).

High-low ohm Low ohmic substrate (10^{18}cm^{-3}), where the bulk is heavily doped as compared to its epilayer.

Low-high ohm High ohmic substrate with a relatively high conducting sheet of Pwell region on top of the epilayer.

6.4.1 Single substrate contact

Let us assume that there is only one single substrate contact on the entire silicon die and this substrate contact is subjected to CDM stress. It is similar to a block of silicon being charged and suddenly discharged through a small contact as shown in figure 6.5. Figures 6.6, 6.7 and 6.8 show the potential drop across the substrate nodes of the silicon with respect to the discharged contact for the three different substrate types. This potential drop distribution is given at a particular time of CDM discharge "t" corresponding to I_{peak} of I_{SUB}. For the high-ohm and low-high ohm substrate, we see a gradual increase in the potential drop at substrate nodes away from the grounded substrate contact. This indicates that as the distance from the substrate contact increases, the probability of CDM failure from voltage overshoot across the substrate and circuit elements also increases. But of course the actual damage location

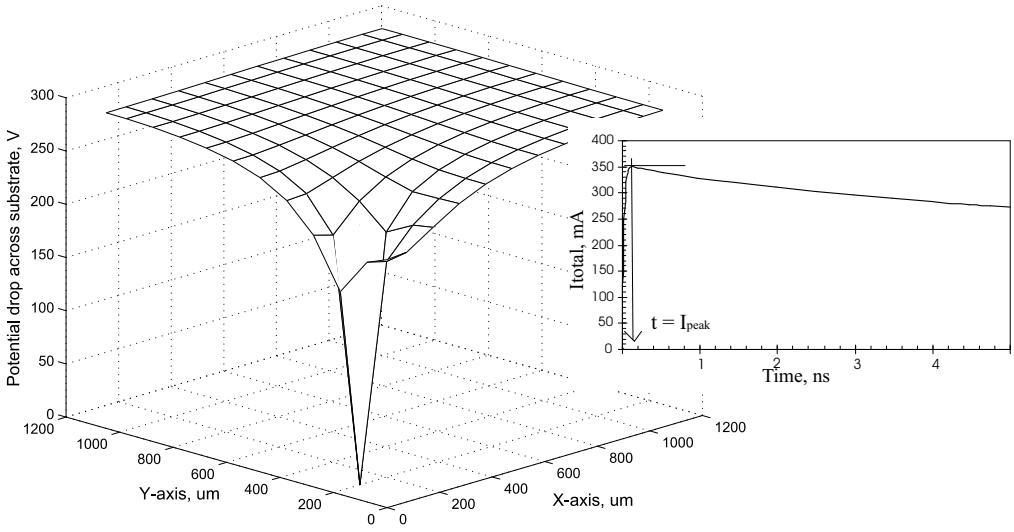


Figure 6.6: Potential distribution across the substrate with a single substrate contact for high-ohm substrate.

will depend on the presence of vulnerable circuit element to CDM failure and its voltage level $e.g.$ gate of a thin gate-oxide MOS. In the case of high-low ohm substrate, all the substrate nodes are at one potential, while the grounded node is at zero (See figure 6.7). This is because the substrate being a highly conducting medium does not allow any significant lateral potential drop across it. As a result, there is no distributed discharge current path for C_{SUB} and the potential drop seen at all the other nodes is simply the IR drop across resistance along the z-direction in the epilayer of the grounded contact. Thus the danger of CDM damage from substrate overshoot is very much small in the circuits built on low ohmic substrate. These potential drop distribution should be seen as the additional voltage drop seen at each substrate node over the voltage drop across the protection device. For a gate-oxide thickness of 7nm, the breakdown voltage is $\approx$ 17V for 1ns stress time. Assuming a potential drop of 7V across the protection device, an additional drop of 10V from the lateral distribution of C_{SUB} discharge current through the substrate can very well result in gate-oxide failure. The substrate voltage can also result in the unwanted turn-on of MOS transistors within the circuit resulting in thermal failure.

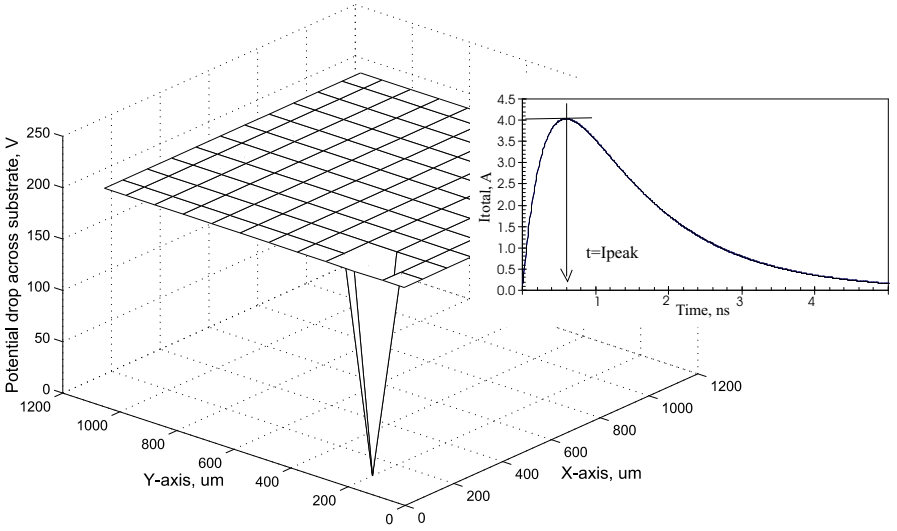


Figure 6.7: Potential distribution across the substrate with a single substrate contact for high-low ohm substrate.

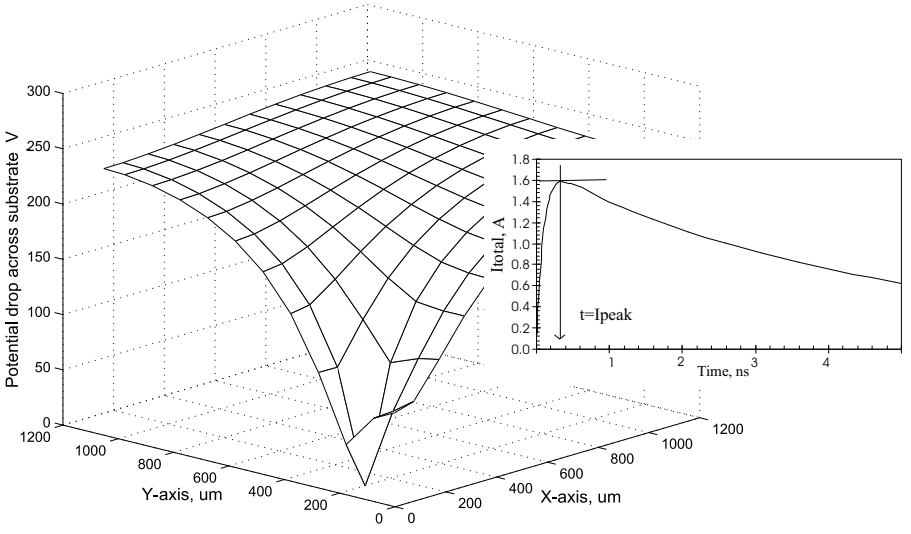


Figure 6.8: Potential distribution across the substrate with a single substrate contact for low-high ohm substrate.

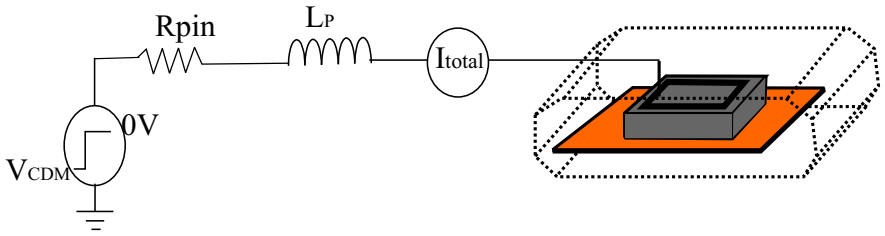


Figure 6.9: Overview of Silicon die with a ring of substrate contact is subjected to CDM stress.

6.4.2 A ring of substrate contacts

Instead of a single substrate contact, let us consider a ring of substrate contacts on the silicon and the substrate contact to be grounded as shown as in figure 6.9. Figure 6.10,figure 6.11 and figure 6.12 shows the simulated potential drop distribution across the three types of substrates, namely high-ohm, high-low ohm and low-high ohm. From the figures we see that the potential drop across the substrate is greatly reduced with a ring of substrate contacts as compared to the single substrate contact. For the high-low ohm substrate, increase of substrate contacts implies reduced effective resistance. This is reflected in the highly oscillating nature of discharge current with very large amplitude 10A and in the potential drop between other nodes and the grounded nodes being reduced from more than 200V to less than 20V as the substrate contacts are increased. Also the extent of reduction is higher for low-high ohm substrate as compared to the high-ohm substrate. This is directly related to the relatively high conducting nature of the Pwell sheet. But of course we haven't included the other parasitic contacts in the silicon and hence the simulated potential distribution can be highly exaggerated as compared to a realistic case. However, from these simulations we can conclusively state that **"By increasing the density of substrate contacts and clever distribution of them across the silicon die, the threat to gate-oxide failures from substrate voltage overshoot can be reduced. Alternately, the danger to gate-oxide failure from excess voltage overshoot of substrate as compared to its gate can be highly reduced is we choose a low ohmic or highly conducting substrate"**

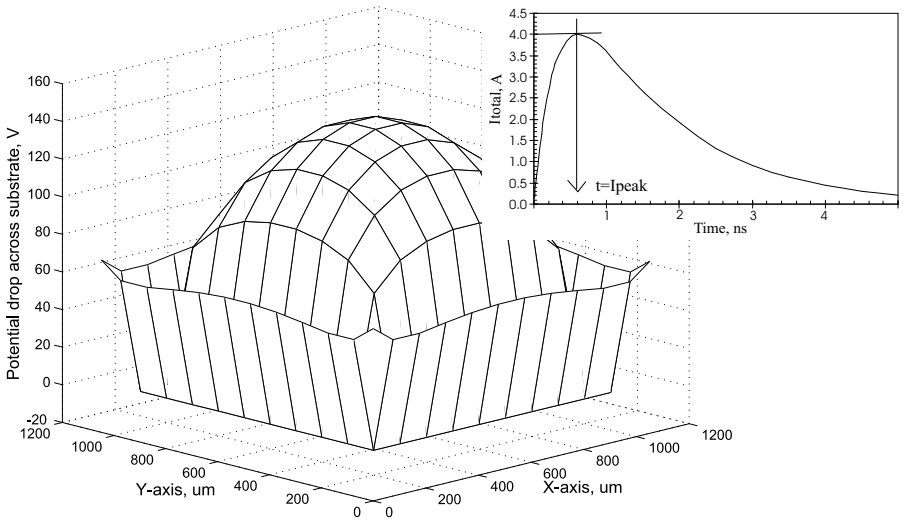


Figure 6.10: Potential distribution across the substrate with a ring of substrate contact for high-ohm substrate.

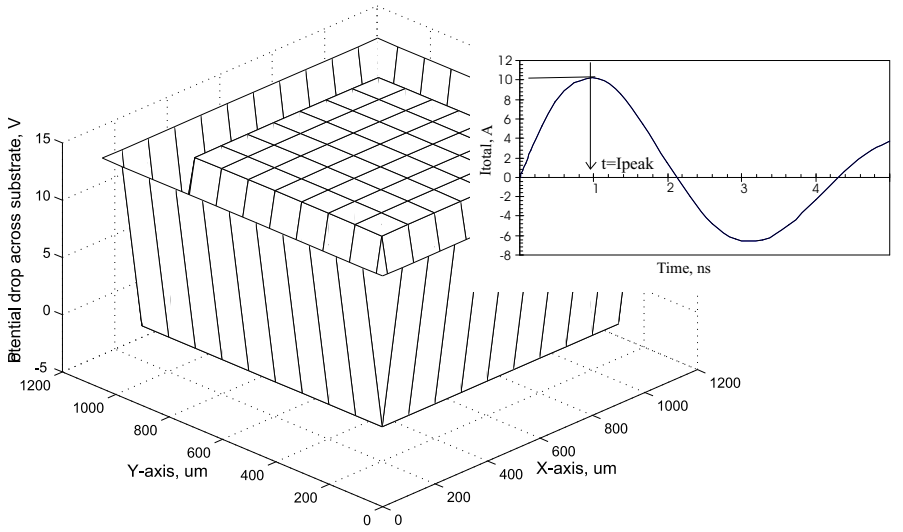


Figure 6.11: Potential distribution across the substrate with a ring of substrate contact for high-low ohm substrate.

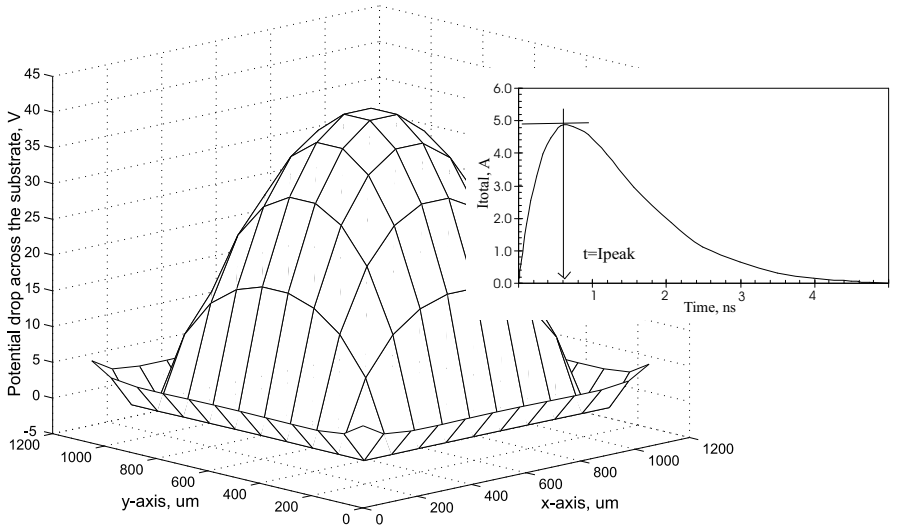


Figure 6.12: Potential distribution across the substrate with a ring of substrate contact for low-high ohm substrate.

6.4.3 Substrate contact distribution in realistic case

We have seen that the P^+ substrate contact distribution can have a significant effect on the excess potential seen by the substrate as compared to its source. In order to design an efficient substrate contact distribution, one should know how the P^+ contact distribution is implemented in the actual circuitry; what are the locations that are likely to face substrate voltage overshoot; and what are the design parameters that needs to be modified. It is interesting to know that there are no separate substrate contacts for each single transistor in a circuitry. Instead the circuits are surrounded by a ring of substrate contacts known as guard rings as shown in figure 6.13. Such a layout is more compact than a layout with many individual contacts to the well. This is done to make the maximum benefit of the underlying substrate common to all these circuits in the third dimension. A guard ring is formed using the N^+ contacts on the Nwell for PMOSts and P^+ contacts on the p substrate for NMOSts to which the substrate connections are made. Hence the potential at any substrate node during CDM discharge will depend on the potential drop between that node and the nearest guard ring or substrate contact. The danger of voltage overshoot across substrate and gate nodes depends on the following,

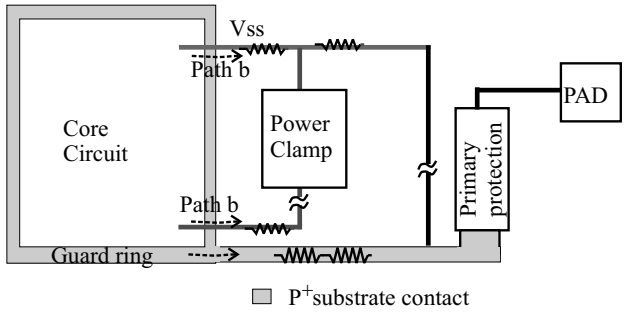


Figure 6.13: Schematic sketch showing the relative positions of the circuit to be protected, the protection devices and the distribution of P^+ contacts.

- **The area enclosed by guard ring.** The larger the area, the larger would be the substrate resistance and larger fraction of C_{SUB} would discharge through it resulting in a larger potential drop.

- **The width of the guard ring.** The width of the guard ring relates to the impedance of the discharge path. Hence the thicker the guard ring, the lower is the impedance and hence the better is the efficiency of the guard ring.

- **Effective $C_{\mathbf{SUB}}$ discharging through a guard ring.** One should be aware of the amount of C_{SUB} discharging through the substrate contacts at the guard ring. It is not only the silicon inside the guard ring area discharging into it but also substrate outside the guard ring. As a result, the potential drop distribution at the substrate node inside the guard ring can change even if the area of the guard ring is constant, depending on the amount of silicon external to the guard ring discharging through it. Consider a silicon block with guard ring as shown in figure 6.14. The potential distribution within the guard ring for high-ohm and low-high ohm substrate are plotted for different values of "*a*" in figure 6.15 and figure 6.16 respectively, "*a*" being excess silicon volume outside the guard ring. From the figures we see that the potential drop within the guard ring increases with the amount excess silicon discharging through it and what differs between the two substrates is the amplitude of the potential drop.

- **Bus line resistance of the substrate rail.** Last but not least, is the potential of the guard ring itself, which depends on the voltage drop across

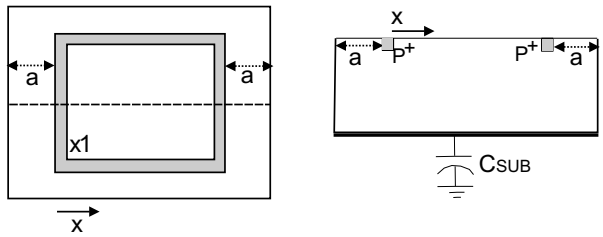


Figure 6.14: Top view of a piece of silicon with guard ring used for simulating figure 6.15 and figure 6.16.

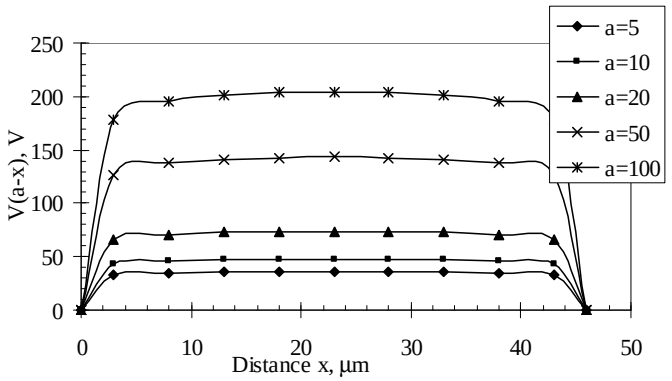


Figure 6.15: Potential drop of the substrate nodes within the guard ring with respect to guard ring potential for different values of "*a*" in Type-a substrate.

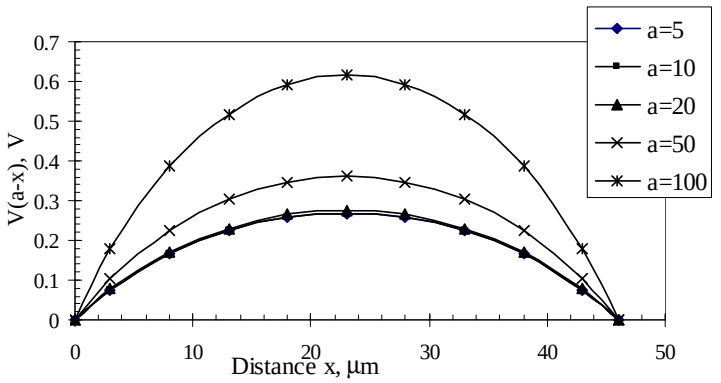


Figure 6.16: Potential drop of the substrate nodes within the guard ring with respect to guard ring potential for different values of "a" in Type-c substrate.

the bus line of the substrate rail from the conducting protection device. Substrate rail is also referred as ground line by design engineers. The metal line connecting the P^+ contacts are in the first metal layer and have large aspect ratio[1]. Width of these bus lines are approximately 1μm. As a result, even if the sheet resistance of the metal line is very low ($\approx$ 100mΩ) a metal length of 50μm can give a resistance of 5Ω. The effective resistance of the V_{SSI} or V_{DD} metal layers is much lesser as they are sheets of metal lines with low aspect ratio. But we know that metal lines connected to the P^+ substrate contacts are the major CDM current path. Hence large resistance associated with these metal lines can greatly degrade the effectiveness of the guard ring protection.

With the trend towards high ohmic substrate to decrease the substrate noise coupling, one would expect the danger from voltage overshoot across the substrate-gate nodes to increase drastically requiring very dense distribution of P^+ substrate contacts. In some of the substrates used in the CMOS technology where deep trench isolations are not present, there is a relatively low conducting (or high doped) Pwell or Nwell region present just below the circuit elements extending until the respective guard ring contacts. But Pwell is not a layer of uniform thickness because of the presence of isolation layers. It is thicker at locations of the the nMOSt and thinner at other locations like below the field oxide. Thinner refers to higher sheet resistance. In which case the actual substrate will be somewhere between high-ohm and low-high ohm.

6.4.4 Meshing Criteria

A proper choice of grid size is an absolute necessity for reduction in the resistive network without having to sacrifice the accuracy of the simulation result. P^+ substrate contacts being the major discharge current path for C_{SUB}, the locations close to the substrate contact are more likely to see maximum potential gradient. Consider a volume element of silicon, both sides of which have P^+ contacts and are grounded as shown in figure 6.17. The number of grids between these two P^+ contacts are varied and the potential drop along its length at a particular time during discharge is plotted in figure 6.17. From figure 6.17 we see the potential gradient is maximum near the grounded edge and minimum towards the center where there is no ground contact. Thus by having dense grid size (maximum resolution) close to the region of maximum voltage gradient and sparse elsewhere, we can achieve a good accuracy with

[1] aspect ratio - ratio between the length and width is large

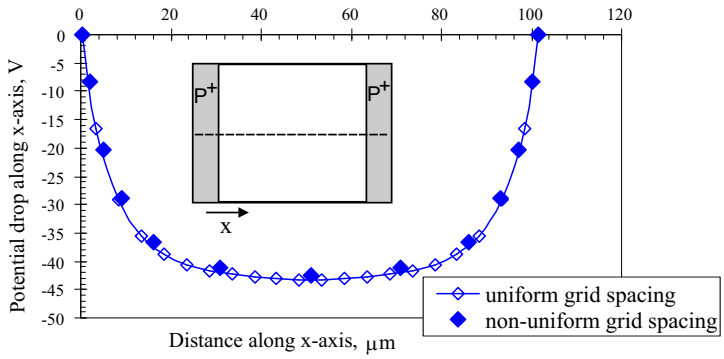


Figure 6.17: Potential drop across the substrate nodes within a guard ring area for different grid size. The inset shows the top view of the silicon where the P^+ contacts are placed.

fewer components. The empty diamond symbols correspond to the voltage distribution across the silicon when the grid size is 5μm throughout the entire silicon block, while the solid diamond symbols correspond to voltage distribution when the grid size is varied from 2μm near the grounded edge to 20μm near the center. From figure 6.17, we see that we can achieve almost the same resolution by proper choice of grid size, with reduced number of unit cells. In the full 3D simulation where we need a resolution of 1μm to 2μm at the certain location of interest and the total die size to be modelled is $\approx 1000\mu$m.1000μm, proper choice of grid size helps in reducing the size of the resistive network by few orders of magnitude. Hence to apply the modelling strategy effectively, we need a prior knowledge on the distribution of substrate contacts (regions of maximum voltage gradient) in the circuit layout. In short, this whole substrate modelling exercise is an attempt to do device simulations on a large scale (entire circuit design).

6.5 Conclusions

Among the various CDM current sources, the capacitance formed by the die attachment plate and the package, C_{SUB} is the largest in magnitude. Moreover the substrate connected to this plate being common to all the circuit elements provides innumerable number of discharge current paths for C_{SUB}. A discharge of C_{SUB} not only causes voltage transients across the gate and source

nodes but also across the gate and its substrate. The probability of gate-oxide failure from the excess voltage overshoot of substrate as compared to its source is investigated with the 3D equivalent circuit model. The various design aspects which can affect the substrate voltage overshoot are discussed.

7 Chapter
Full Chip Circuit Model - 1

This chapter presents a practical application of the 3D full chip CDM circuit model. The two ICs modelled are I/O test structures in 0.18μm technology with pad based protection with slightly different protection designs. CDM measurements on these test structures showed significantly large variation in their threshold level. In this chapter, using our new model, the effect of the design variation on the voltage transients across the gate-oxide of the MOS transistors in the input buffer for the two ICs are investigated for different substrate contact distribution with the power lines.

7.1 Introduction

The input buffers are one of the most vulnerable locations to CDM failure because the gate of these devices are directly connected to the grounded pad. This is also the reason why most of the ESD protection circuits are mainly focussed towards developing a robust I/O protection design. In chapter 4, we have discussed in detail the various design criteria for an efficient I/O protection design when the substrate and the source nodes of the MOS transistors in the circuit to be protected, are shorted. In the protection design investigated in this chapter, the substrate and source nodes are not necessarily at the same potential. Hence the danger of gate-oxide failure from voltage overshoot between the gate and substrate nodes of the MOS in the input buffer of the two ICs are studied. Additionally the influence of increasing the substrate contact distribution with the V_{SS} on the gate-substrate voltage across the MOS in the input buffer is investigated.

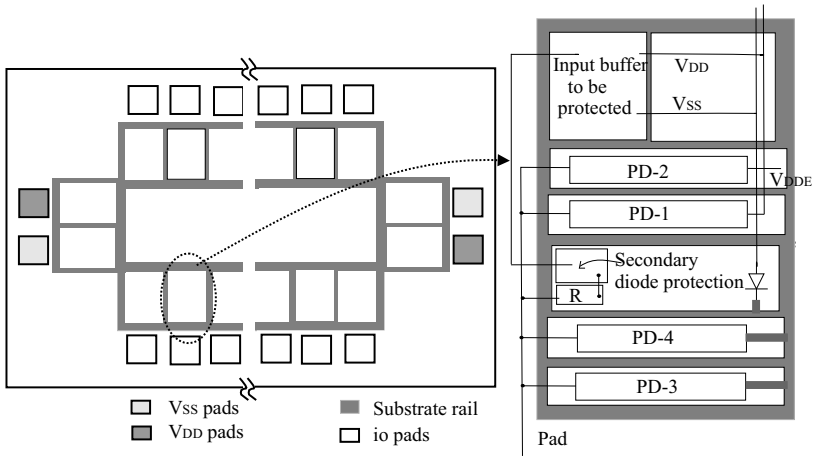


Figure 7.1: Layout of the IC showing the distribution of the protection devices within an input cell.

7.1.1 IC Description

The two IC designs under study are I/O ring test structures in the 0.18μm technology node housed in a CDIL40 pin packages. In both the IC designs, the protection is pad based, wherein each I/O pad is connected to the power lines via one or more protection devices. The layout of the circuits in both the designs are similar to each other and is as shown in figure 7.1. The subset of the figure shows the distribution of the protection devices and the circuit to be protected. The circuit to be protected is an input inverter. Let us call the two protection designs as original and improved designs. The schematic of the protection designs in the two ICs, original and improved are shown in figure 7.2 and figure 7.3 respectively. Both the IC designs have the same package type, die size, pin counts and the same layout for the primary protection devices at the I/O pads. The improved design varies from the original in,
1) Presence of the additional protection devices PD5 and PD6 connected to the same power lines as that of the input buffer (circuit to be protected);
2) Higher value of the decoupling resistance;

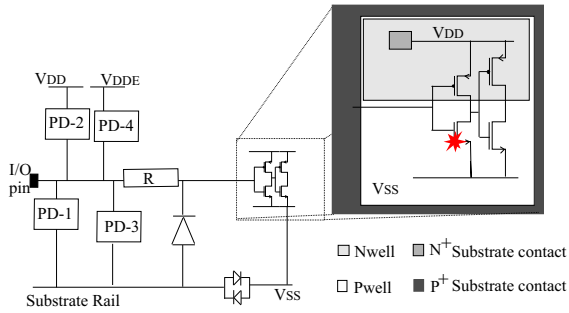


Figure 7.2: Schematic sketch of the input protection design in design1 (original).

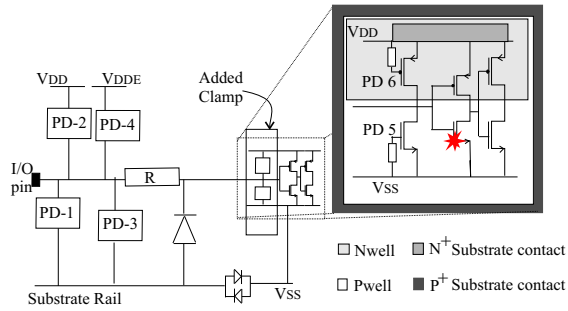


Figure 7.3: Schematic sketch of the input protection design in design2 (improved).

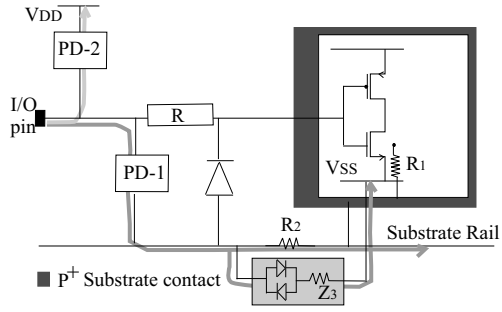


Figure 7.4: Simple schematic of an I/O cell.

7.1.2 CDM Measurement Results

Field Induced CDM measurements were done on both the ICs. You can find a detailed description of the CDM measurement procedure in chapter 3. Those ICs with design1 had a maximum CDM threshold level of $-400V$ only, while those with design2 did not fail even at $-1000V$ CDM stress. Failure analysis on the failed ICs with design1, showed gate-oxide failure at the first input buffer, whose gate is directly connected to the input pad. The failure location was generally at the NMOS gate and only occasionally at the PMOS gate.

7.1.3 Discussion

During CDM stress of any I/O pin of an IC, C_{SUB} discharges mainly through the P^+ substrate rails and the power lines connected to the discharged pad via protection devices. The amount of discharge current carried by these lines on the event of CDM stress depends on the type of connection these lines make with the substrate. Finally all the CDM current from these metal lines flows out through the protection device of the corresponding grounded pin. We have shown earlier in chapter 5, that **"it is not the CDM current but the voltage transients across the device arising from the ESD current flow which causes the gate-oxide failure"**. The CDM current flowing through an input protection circuit when subjected to negative CDM stress is shown in figure 7.4. The voltage drop between the gate and source nodes of the NMOS in the input buffer is given by,

$$V_{\text{gate}} - V_{\text{source}} = V_{\text{Z3}} + V_{\text{PD-1}} \tag{7.1}$$

where,
V_{Z3} - Potential drop along the V_{SS} line between the source contacts of the NMOS and its contact to the substrate rail.
$V_{\text{PD-1}}$ - Potential drop across PD-1.
In the presence of an additional clamping device, as in design2, the maximum voltage drop seen between the gate and source nodes of the NMOS is limited by the snapback/turn on voltage of the added clamping device.

$$V_{\text{gate}} - V_{\text{source}} \leq V_{\text{snapback}}(PD-5) \tag{7.2}$$

The excess voltage drop above the clamping voltage of the primary protection device, seen across the gate and source nodes of a NMOS depends on the amount of CDM current flowing through Z3. The danger to gate-oxide failure

is directly related to this excess voltage drop seen across the gate-oxides. Thus the presence of additional protection device would cause a significant improvement in the CDM robustness of the design, if the current flowing through $Z3$ is large. The reasoning holds the same for PMOS in the input buffer.

Voltage transients across the gate and the power lines is just one side of the story. Gate-oxide failures can also result from voltage overshoots across the gate-substrate nodes of the MOS. Generally it is assumed that the source and the substrate are at the same potential. But this is not true. The voltage drop between the gate and substrate node of an NMOS is given by,(See figure 7.4)

$$V_{\text{gate}} - V_{\text{substrate}} = V_{\text{R1}} + V_{\text{R2}} + V_{\text{PD-1}} \tag{7.3}$$

where,
V_{R1} - Voltage drop between the substrate node of the MOS and the nearest P^+ substrate guard ring
V_{R2} - Voltage drop along the P^+ substrate rail between the guard ring and its contact with the V_{SS} line near the primary protection device location.
From equation 7.1 and equation 7.3, we get the voltage drop between the source and substrate node of the NMOS in the input buffer as,

$$V_{\text{substrate}} - V_{\text{source}} = V_{\text{R1}} + V_{\text{R2}} - V_{\text{Z3}} \tag{7.4}$$

To keep the source and substrate nodes at the same potential,

$$V_{\text{R1}} + V_{\text{R2}} = V_{\text{Z3}} \tag{7.5}$$

This can be done by routing maximum amount of discharge current to flow along V_{SS} through Z3.

The decoupling resistor reduces the transients as seen by the gate-oxide, before the primary protection device turns on and helps in limiting the current flowing through it. As the influence of decoupling resistor on the CDM performance of an I/O protection circuit has already been studied extensively in chapter 3, we limit our discussion in this chapter to the influence of the added clamp on the CDM performance alone.

Presence of the additional protection devices within the same guard ring region where the circuit to be protected is placed reduces the voltage drop across the source and substrate nodes of the MOS. The added protection device is a ggNMOS (ggPMOS). As this protection device turns on, the diode between the source and substrate nodes of the protection device gets forward biased and thus potential at the substrate node of the added protection device is brought

closer to its potential at the source. As a result, the potential at the substrate node of the MOS to be protected will also be reduced, depending on its *effective distance* from the added protection device. Thus if the added protection device is placed closer to the MOS to be protected and clamped to the same power lines, the voltage transients across both gate-substrate and gate-source nodes of the MOS will be lowered. But the improvement in the CDM withstand level brought by the added clamp depends on the amount of current conducted through the various lines, which in turn depends on how these power lines are connected to the substrate in a given circuit.

In this chapter, both the IC designs are modelled into 3D circuit network. This 3D circuit model is later used to investigate the influence of the added clamp on the voltage transients seen across the gate-oxides of the input buffer under three different distributions of the power line contacts with the substrate. These power line contacts are present in addition to the parasitic diode contacts which the power lines make with the substrate through the circuits.

One contact: The V_{SS} and V_{DD} lines are shorted to the substrate nodes of the primary protection devices at the input pad subjected to CDM stress.

Contacts at power pads: A short from the V_{SS} line to the substrate at the V_{SS} pad location and a power clamp between the V_{DD} line and substrate at the V_{DD} pad location are also included. This substrate contact distribution is similar to the distribution present in the test structures.

Ring of substrate contacts: A ring of P^+ substrate contacts is added to both the designs and the V_{SS} line is shorted to the P^+ substrate for each 100μm distance.

7.2 Building of the 3D Circuit model

The full chip circuit model as explained in chapter 6 is built in the following stepwise sequence.

Step1: Determine C_{SUB} of the IC and the dimensions of the die.

Step2: Choose the grid size of the resistive network from the overall layout of the circuit with the location of the protection devices and the circuit location in mind. This step is crucial in determining the accuracy

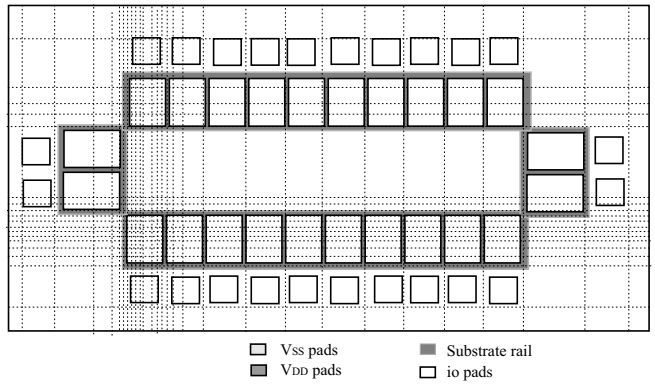


Figure 7.5: Layout of the entire IC in both design1 and design2 along with the grid size used.

of the simulation results. Figure 7.5 shows the layout of the IC and the grid size chosen at different locations of the circuit. Maximum resolution or minimum grid size is provided near the location of the circuit to be studied. The size of the protection devices determine the resolution at other locations.

Step3: Model the substrate rails and power supply line distribution and their contacts with the circuit. These supply lines are common to all the circuit elements and have bus line resistance. The metal line resistance of these supply lines is extracted from the layout. The distributed nature of the power lines is modelled as shown in figure 7.6. The V_{SS} line is connected to the substrate rail near its protection device clamp through antiparallel diodes. This antiparallel diode connection is not effective under CDM stress. The effectiveness of the antiparallel diode is explained discussed in detail in the appendix at the end of this chapter. The antiparallel connection is replaced by a small resistor at the discharged pin location and left as an open at other pin locations. The P^+ substrate contact lines are connected to the source of the protection devices.

Step4: Make the circuit connections with the substrate and the supply lines. The connections which the circuit elements make with the substrate are the discharge paths for C_{SUB}. The main discharge paths are through the P^+ substrate contacts to the discharged pin via the protection devices. Hence the first and important design of the circuit to be modelled is the P^+ contacts and the protection devices connected to

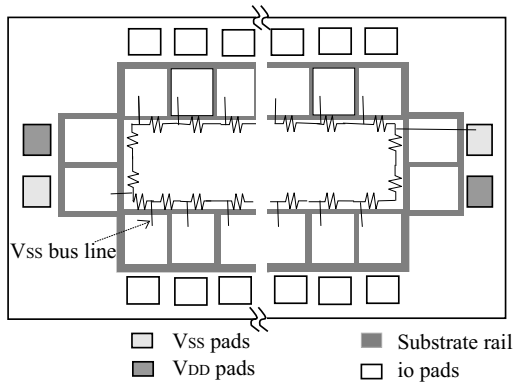


Figure 7.6: Distributed bus line resistance as modelled in the circuit.

it. Next is to include the effect of other circuit elements on the voltage transients across the circuit. The circuit elements are replaced by their equivalent CDM circuit as explained in chapter 6 to model the parasitic contacts between the substrate and the power lines V_{DD} and V_{SS}.

Step6: The parasitic elements of the package like L_{P}, C_{PIN} and the tester parasitic are measured and included in the circuit model.

Thus the entire full chip 3D circuit model of the IC is built. The CDM stress is simulated on the circuit by sudden grounding of the pin corresponding to the input buffer to be studied. The sudden grounding is simulated by V_{SWITCH} going from pre-charged voltage level V_{CDM} to $0V$ in time $t = 100fs$. A detailed explanation on the CDM circuit model is presented in chapter 2.

7.3 Voltage transients across substrate

The two test structures are completely identical to each other when the input protection design is not included. A CDM stress of -300V is simulated on this test structure without including the input buffer circuitry. The voltage drop across each substrate node with respect to the discharged pin at time $t = t_{\text{Ipeak}}$ during the CDM discharge is shown in figure 7.7. t_{Ipeak} is the time at which the current discharging through the circuit is maximum. The presence of P^+ substrate contacts and protection device closer to the I/O pads and no substrate contacts in the central region of the IC design, creates two extreme zones with

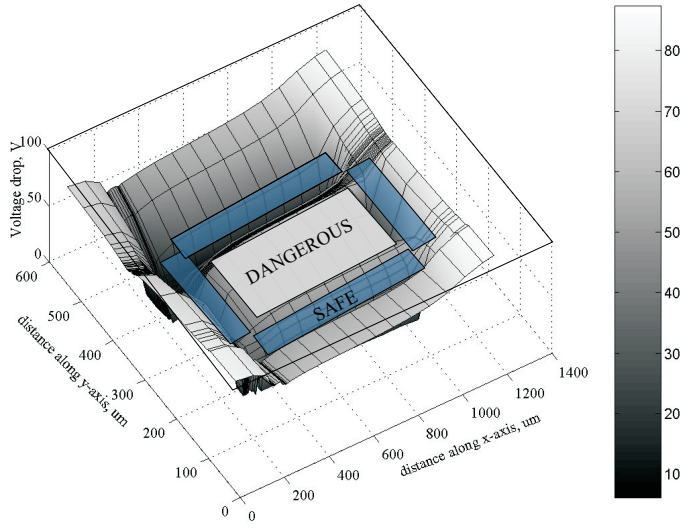


Figure 7.7: Voltage transients across each of the substrate nodes in the IC with respect to the discharged pad at 470ps during -300V CDM stress.

regard to voltage transients during CDM stress. One, the SAFE zone where the substrate is closer to V_{hold} of the protection device and two, the DANGEROUS zone, where the voltage transients at the substrate nodes are much larger than V_{hold}. In the test structures studied, the input buffer to be protected is present in the region between these two zones. Voltage transients greater than the gate-oxide breakdown threshold, seen at substrate nodes can be destructive if the circuit element at those nodes happens to be a gate-oxide capacitor. Thereby it becomes necessary to study the gate-substrate voltage transients across the MOS gates as well.

We limit our analysis to the study of the vulnerability of the MOS at first input buffer to gate-oxide failure. In the following section, we study voltage transients across the gate-source nodes and gate-substrate nodes of the MOSts in the input buffer for different distributions of direct power line V_{DD} and V_{SS} contacts with the substrate rail.

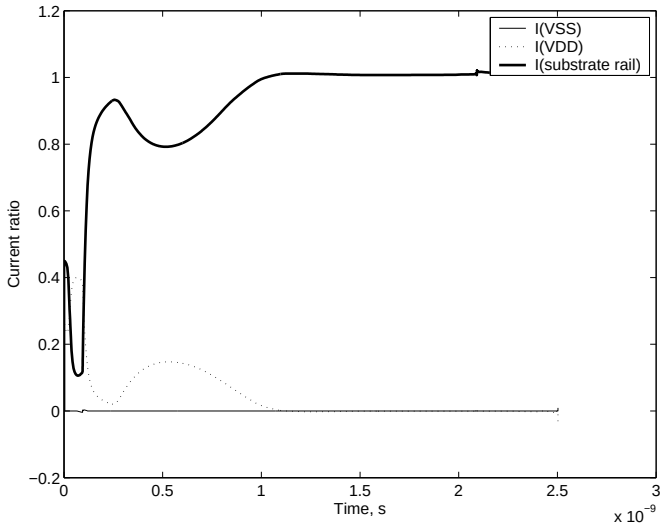


Figure 7.8: Simulated CDM current discharged through the power lines, V_{SS} and V_{DD} and the P^+ substrate rail in the circuit during -300V CDM stress in the test structure with one substrate contact.

7.3.1 One Contact

In this case the substrate is connected to the V_{DD} and V_{SS} lines through the parasitic diode contacts which the MOS in the circuit makes with the substrate. Additionally the V_{DD} is connected to the substrate via parasitic Nwell contacts at the protection device locations at each I/O pad and the V_{SS} line is shorted to the substrate at the protection device location of the grounded input pad. Figure 7.9 shows the discharge current path when the the input pin is subjected to a negative CDM stress. Figure 7.8 shows the relative magnitude of the current flowing through three major discharge current paths namely, the substrate rail, V_{SS} and V_{DD} when the IC is subjected to -300V CDM stress. The current distribution in the three major discharge current paths will be almost the same for both the designs. From figure 7.8 we see that majority of the CDM discharge current flows through the substrate rail. This is because the P^+ contacts shorted to the substrate rail are well spread throughout the die and are also the lowest impedance paths for the discharge of C_{SUB}. As the V_{SS} line contacts the substrate only through the parasitic diode contacts, the ratio of the total discharge current discharged through V_{SS} is very small.

NMOS of Input buffer: The voltage transients seen across the gate and sub-

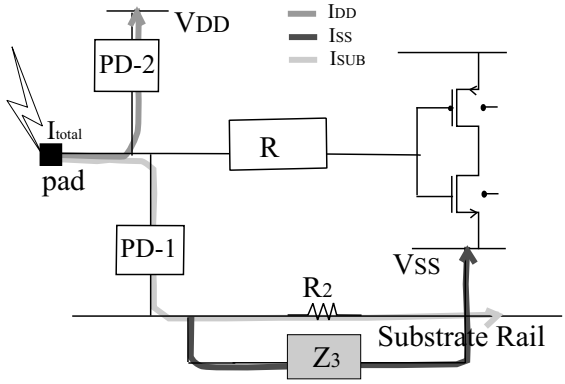


Figure 7.9: The current path through the circuit when an input pin is subjected to negative CDM stress.

strate node and between the gate and the source nodes of the NMOS in the input buffer in two designs are shown in figure 7.10 and figure 7.11 respectively. For reference the voltage drop across the primary protection device PD-1 is also plotted in the figure. From figure 7.10 and figure 7.11, we see that the voltage transients across the gate-source nodes do not rise above the voltage drop across the primary protection while the voltage drop across the gate-substrate node rises around 10V higher than that across the primary protection. This is because most of the CDM current is being conducted via the substrate rail and not through the V_{SS} line. As the amount of current conducted through V_{SS} is very small, the corresponding voltage drop along this line V_{Z3} is also small. Thus the design without the additional protection device poses no threat to gate-oxide failure with respect to voltage transients across gate-source nodes while a large threat with respect to voltage transients across gate-substrate. In the presence of the additional protection device, we see a drop in the potential across the gate-source nodes of the NMOS. This is because the primary protection device and the added protection device do not have the same turn-on voltage level. The added protection device in the improved design is a gate coupled NMOS and has a gate length of 0.18μm. While the primary protection device is a ggNMOS with gate-length 0.52μm. Thus the added protection device has a lower turn-on voltage than the primary protection because of the gate-coupling effect. The reduction in the voltage drop across the gate and source node of the NMOS depends on the amount of current conducted through the decoupling resistor. When the protection device turns on, it pulls its substrate potential closer to its source potential V_{SS}.

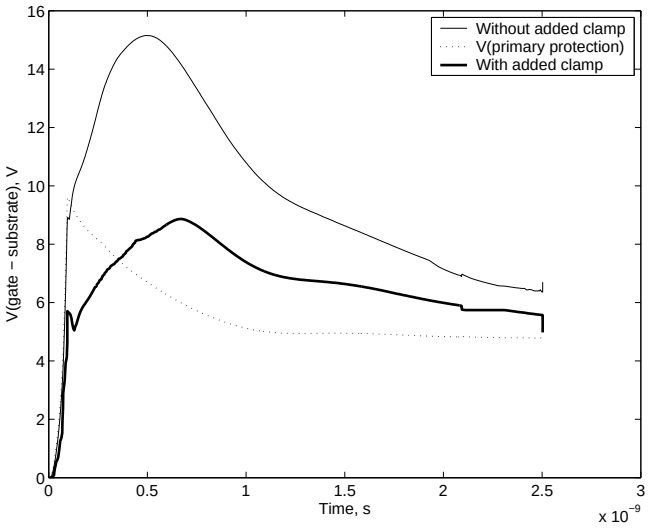


Figure 7.10: Simulated voltage transients across the the gate and substrate nodes of the NMOS in both the designs during -300V CDM stress in the test structure with one substrate contact.

The presence of protection device closer to the device to be protected reduces the voltage overshoot across the gate and substrate nodes of the MOS as well. The reduction in the voltage overshoot across the gate and substrate nodes of the MOS depends on its effective distance from the substrate node of the added protection device. In the design without the additional clamp, the voltage transients across the gate and substrate nodes exceed much higher than the holding voltage of the primary protection device. The presence of the additional clamp closer to the device to be protected reduces this excess voltage overshoot and thereby improves the withstand level of the design. With respect to the voltage transients across the the gate and source nodes of the NMOS, $V_{\text{gate-source}}$ is almost equal to the holding voltage of the primary protection in the design without the additional clamp and thus poses no danger to gate-oxide failure. Hence if we consider only the $V_{\text{gate-source}}$ voltage transients, we will not be able explain the observed improvement in the withstand level of the protection design with the added clamp.

PMOS of Input buffer: Figure 7.12 and Figure 7.13 shows the voltage transients seen across the gate-oxide of the PMOS in the input buffer during -300V CDM stress. From figure 7.10 and figure 7.12, we see that the voltage transients seen across the gate-oxide of the PMOS is less than that of the

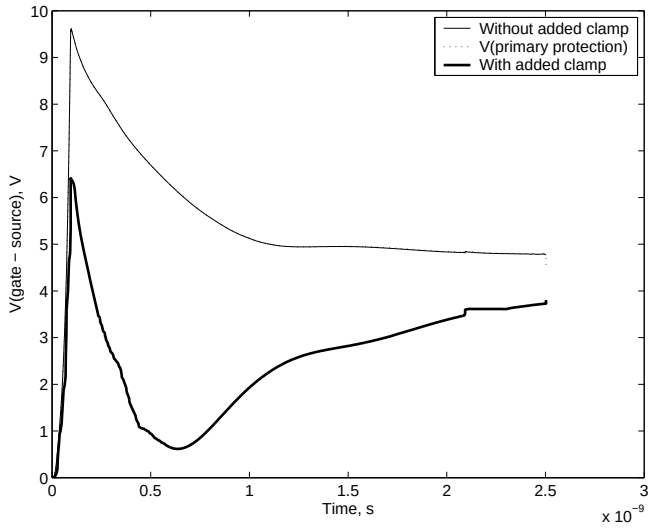


Figure 7.11: Simulated voltage transients across the gate and source nodes of the NMOS in both the designs during -300V CDM stress in the test structure with one substrate contact.

NMOS. This is because, during negative CDM stress, it is the parasitic diode of the primary protection to the V_{DD} line that turns on, while it is the L-BJT (Lateral Bipolar Junction Transistor) of the primary protection to the substrate rail that turns on for most period of the stress and vice versa during positive CDM stress. The voltage drop across the gate-source nodes of PMOS does not rise much above voltage transients across its primary protection device, even though there is considerable amount of current conducted through the V_{DD} line (See figure 7.8). This is because of the small bus line resistance value used to model the resistance of the V_{DD} line between the source of PMOS and the primary protection. The reason for the small value used is because the N^+ contact to the Nwell of the PMOS is shorted to the V_{DD} line.

The voltage overshoot of the substrate node of the PMOS above V_{DD} depends its effective distance from the N^+ substrate contact and the amount of discharge current conducted through the Nwell. The presence of additional protection device, PD-6, reduces the voltage overshoot further in a similar manner as in NMOS. As the voltage transients across the gate-oxide of the PMOS is much less than that of the NMOS during negative stress and as the influence of the design variations are the same for both the MOS, we will limit ourselves to the study of voltage transients across the gate-oxide of the NMOS alone in the

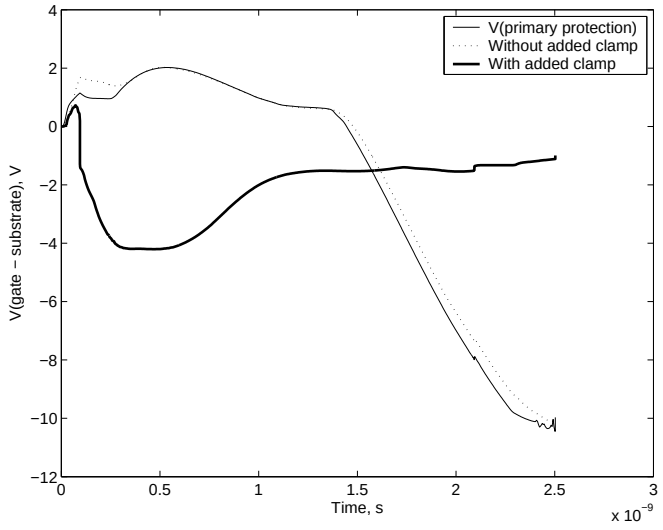


Figure 7.12: Simulated voltage transients across the gate and the substrate nodes of the PMOS with and without the presence of additional clamping device, under -300V CDM stress.

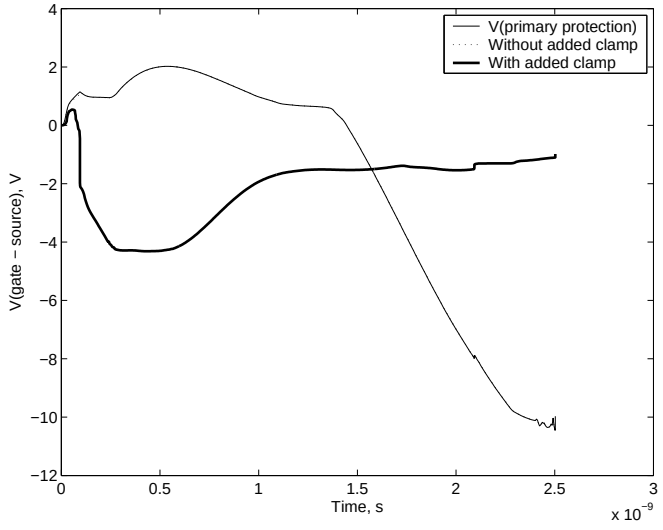


Figure 7.13: Simulated voltage transients across the gate and the source nodes of the PMOS with and without the presence of additional clamping device, under -300V CDM stress.

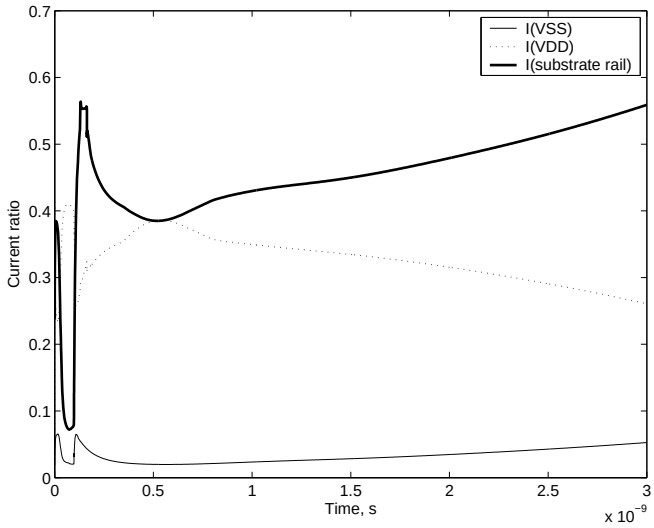


Figure 7.14: Simulated CDM current conducted through the different power lines in the circuit during -300V CDM stress, when the power clamps across the V_{SS} and V_{DD} line and the substrate line are included.

following sections.

7.3.2 Contacts at power pads

The additional contacts presented in this case is the short from the V_{SS} line to the substrate rail at V_{SS} pin location. Also the V_{DD} lines are clamped to the substrate rails via power clamps (snapback devices) at V_{DD} pin location. On including these contacts in the circuit, the current transients across the various power lines get modified. The ratio of the total CDM current discharged through the bus lines V_{DD}, V_{SS} and substrate rails is as shown by in figure 7.14. From the figure we see that by shorting the V_{SS} line to the P^+ substrate contact, the ratio of CDM current discharged through the V_{SS} line is increased and that through the substrate rail is decreased. This is because P^+ substrate lines are narrow metal lines present in the first metal layer and hence have much larger effective resistance ($\approx 1\Omega/10\mu$m) when compared to the V_{SS} and V_{DD} line ($\approx$ 120m$\Omega/100\mu$m) which is a metallic sheet. As a result, more of the CDM current flows from substrate rail into the V_{SS} line. Similarly the current through the V_{DD} line is also increased by including the inter power clamps across the P^+ substrate rail and the V_{DD}. The voltage transients across the

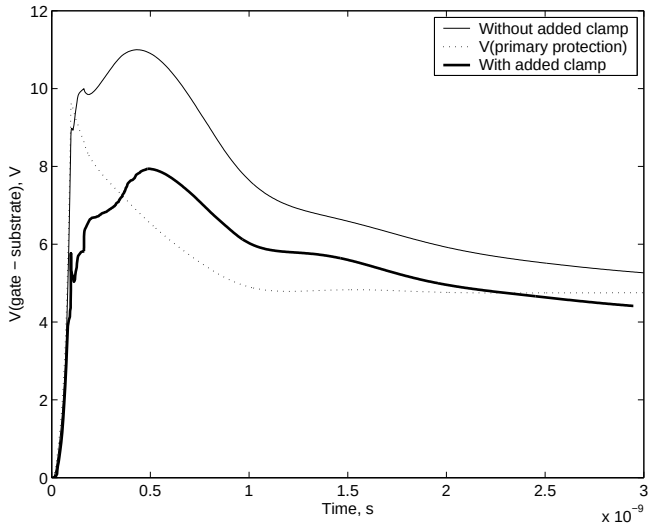


Figure 7.15: Simulated voltage transients across the gate and the substrate nodes of the NMOS with and without the presence of additional clamping device under -300V CDM stress, when the power clamps across the V_{SS} and V_{DD} line and the substrate line are included.

gate-oxide of the NMOS in the two designs in this case is shown in figure 7.15 and figure 7.16. With increased current flowing through the V_{SS} line, we see the voltage transient across the gate-source nodes of the NMOS rises above the holding voltage of the primary protection in design1, depending on the voltage drop V_{Z3} along the V_{SS} line. In the presence the additional clamping device, the voltage transient seen across the gate-source nodes is lower than the voltage drop across primary protection depending on the amount of current conducted through it.

The increase in current flow through the V_{SS} line results in the increase of V_{Z3} in equation 7.4. As a result, $V_{\text{gate-substrate}}$ across the NMOS is reduced as compared to its transients in the design with one substrate contact. But $V_{\text{gate-substrate}}$ of NMOS is still much higher than its $V_{\text{gate-source}}$ transients. In the presence of the additional protection device, there is further reduction in $V_{\text{gate-substrate}}$ across the gate-oxide of the NMOS. With increase in the discharge current conducted through V_{SS} line, the additional protection device plays a considerable role in ensuring that the voltage overshoot across the gate and source nodes are well clamped. But it does not guarantee the voltage transients across the gate and substrate nodes to be within the holding voltage of the added clamp. This is

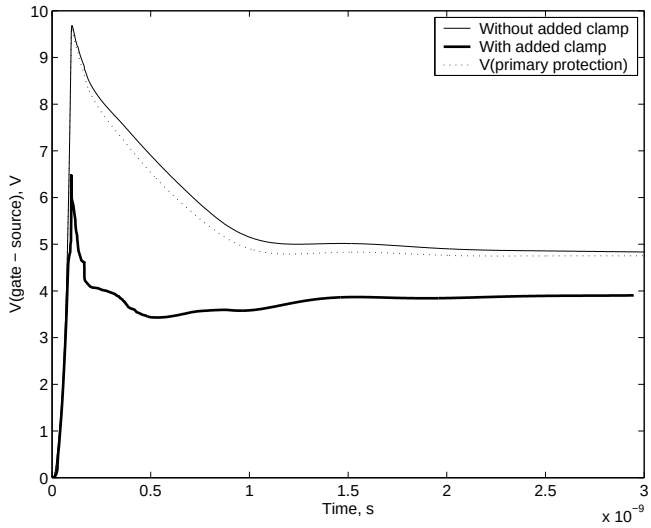


Figure 7.16: Simulated voltage transients across the gate and the source nodes of the NMOS with and without the presence of additional clamping device under -300V CDM stress, when the power clamps across the V_{SS} and V_{DD} line and the substrate line are included.

because locally the substrate discharges through its nearest P^+ substrate contacts and during CDM discharge the P^+ substrate contacts near the device to be protected can be at quite a different potential from that of the V_{SS} line.

7.3.3 Ring of substrate contacts

Let us take the analysis one step further and include a ring of P^+ substrate contacts as shown in figure 7.17 and locally short substrate rails to the V_{SS} lines at each pin location. The ratio of the CDM current conducted through the bus lines V_{SS}, V_{DD} and substrate rail is shown in figure 7.18. The figure shows that the current conducted through the V_{SS} line is increased even much higher than the CDM current discharged through its substrate rail. But there is a slight drop in the amount of current conducted through the V_{DD} line. This is because the substrate from the Nwell region discharges through the substrate into the nearest P^+ substrate contact instead of flowing through the Nwell into the V_{DD} line. Figure 7.19 and figure 7.20 shows the voltage transients across the gate-substrate and gate-source nodes of the NMOS during the CDM stress. From the figure we see that the voltage transients across the gate and source

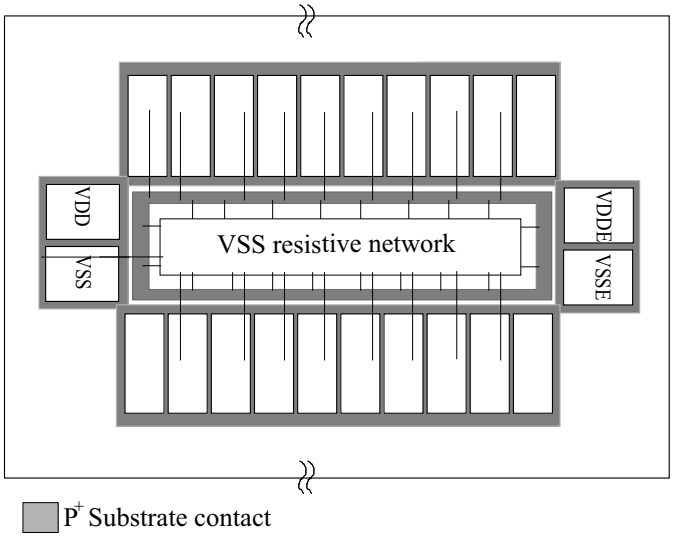


Figure 7.17: Layout of the IC with additional P^+ substrate ring and well shorted to the V_{SS} line.

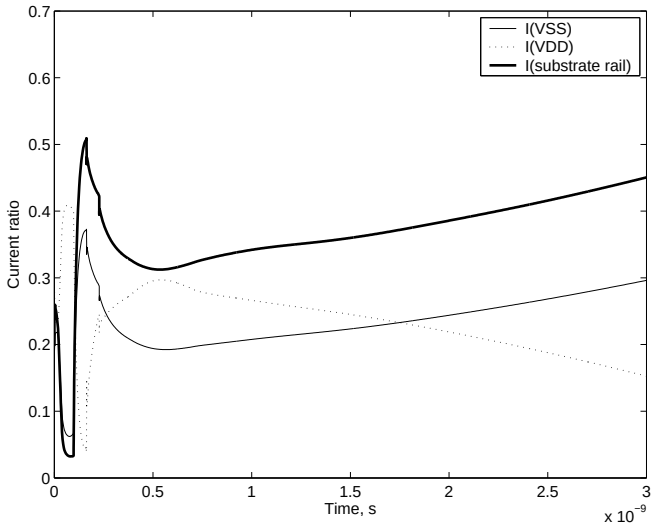


Figure 7.18: Simulated CDM current conducted through the different power lines in the circuit during -300V CDM stress, with additional ring of P^+ substrate contacts connected to the V_{SS} line.

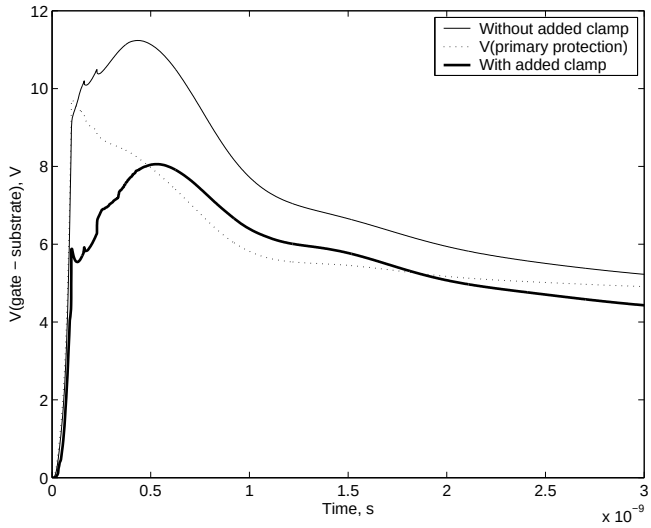


Figure 7.19: Simulated voltage transients across the gate and substrate nodes of the NMOS with and without additional clamp under -300V CDM stress, with additional ring of P^+ substrate contacts connected to the V_{SS} line.

nodes exceed much higher than the holding voltage of the primary protection. The presence of additional protection device, plays significant role in ensuring that the voltage overshoot across the gate and source nodes is well clamped. In this case, the design with additional clamp certainly improves the CDM withstand level of the circuit with respect to voltage transients across the gate and source nodes. On locally shorting the substrate rails to the V_{SS} line, the ESD current flowing through the P^+ substrate rail is decreased resulting in a large reduction of the voltage difference between the source and substrate nodes of the NMOS.

From the above analysis, we can conclude that the added clamp causes a significant improvement in the robustness of the design only if most of the CDM current is directed into the V_{SS} and V_{DD} lines. But one should not forget, that this added clamp has to be designed as close as possible to the circuit to be protected, which places a limitation on the size of the added clamp and hence on the amount of current conducted through it. For the overall improvement in the protection design, the current conducted through the additional clamp has to be limited. Figure 7.21 shows the discharge current conducted through the added clamp for the different distributions of substrate contact. Figure 7.21 shows that the amount of CDM current conducted through the added clamp is

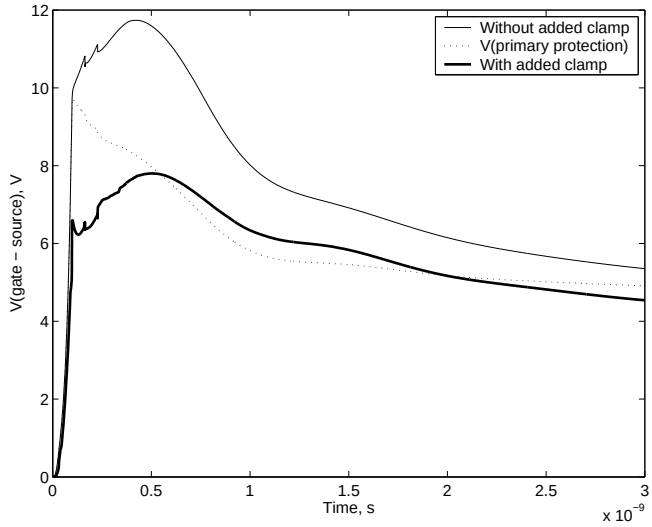


Figure 7.20: Simulated voltage transients across the gate and source nodes of the NMOS with and without additional clamp under -300V CDM stress, with additional ring of P^+ substrate contacts connected to the V_{SS} line.

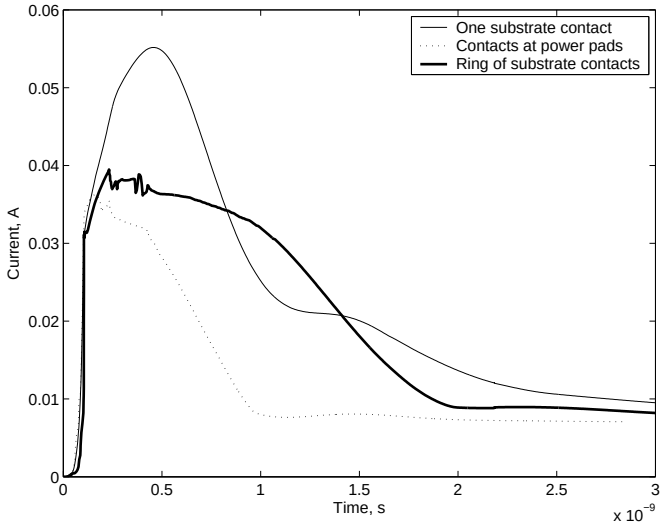


Figure 7.21: Current conducted through the added clamp in under three different substrate contact distributions namely, one substrate contact, contacts at power pads, and additional ring of substrate contacts

decreased with additional substrate contact at the V_{SS} pad. But as the number of substrate rail contacts to the V_{SS} line is increased, the current conducted through the added clamp is also increased. The reason is as follows. With single substrate contact, the current conducted through the added clamp is from its substrate contact. With an additional substrate rail contact to the V_{SS} line, the amount of current conducted through the substrate is decreased. But when the V_{SS} line is well shorted to the substrate rail, most of the current flows through the V_{SS} line rather than the substrate rail. This results in the voltage drop along the bus line (V_{Z3}) to be significant. The additional voltage drop across the bus line forces the added clamp to conduct more current.

7.4 Conclusions

A 3D circuit analysis on the CDM performance of ICs with different I/O protection designs has been presented. CDM gate-oxide failure can result from voltage transients across gate-source nodes and also from gate-substrate nodes of a MOS. This 3D circuit model helps in studying both the voltage transients across the NMOS during CDM stress. The presence of additional protection device ensures the maximum voltage transient across the gate and source nodes to be limited to the trigger voltage of the added clamp, but does not limit the voltage transients seen across the gate and substrate nodes of the MOS. With regard to gate-oxide failure from voltage overshoot across the gate and substrate node, the presence of additional clamp will improve the CDM withstand level provided major portion of the discharge current is conducted through the power rails instead of being conducted through the substrate. This can be achieved by increasing the number of power line connections to the substrate. Thus to avoid gate-oxide failure from voltage transients across the gate and substrate nodes, substrate rails must be locally shorted to the corresponding power lines which are well clamped.

Appendix:

Effectiveness of antiparallel diode connection under CDM stress:
The antiparallel diode connection is not very direct and simple as shown in the schematic circuits (See figure 7.2). In fact the diodes are not of the same dimensions and are also not placed at the same location. One of the antiparallel

diodes is an intentional diode design made in the layout closer to the primary protection. Here the V_{SS} line connects to the Nwell diffusion in the substrate. The other diode is from the parasitic diodes formed by the N^+ source contacts on the p-substrate by the NMOS transistors in the circuit design. Under negative CDM stress condition, the specifically designed diode is reverse biased (substrate rail is more positive than V_{SS}). The parasitic diodes formed by the V_{SS} source line with the p-substrate is also reverse biased (substrate being more negative than V_{SS} line). The effectiveness of the antiparallel diode will depend on how well the substrate nodes are kept close to the substrate rail potential. As the number of V_{SS} line contacts with the substrate is increased, more of the CDM current is discharged through the V_{SS} line and the efficiency of the antiparallel diode connection is improved.

8 Chapter
Full Chip Circuit Model - 2

CDM measurement results on an IC with rail based protection in a 0.12μm technology node, showed gate-oxide failure at MOS in the internal circuitry whose gates are connected to the internal nodes in the circuit and do not see the external world. The voltage transients across the gate-source nodes and gate-substrate nodes of these MOS when subjected to CDM stress and the background for such large voltage overshoots across the gate-oxides are investigated in this chapter with the 3D full chip circuit model. To investigate CDM robustness enhancement, the effect of V_{SS} line contact distribution with the substrate rail and the area of the guard ring inside which the MOS are present, on the gate-oxide voltage transients are studied with the 3D full chip circuit model.

8.1 Introduction

In a rail based protection, each I/O pad is clamped to the power rails via diodes and the all the V_{DD} lines are clamped to their respective V_{SS} lines by very large (width $\approx$ 2mm) MOS transistors known as BIGFET. The protection devices are placed such that CDM current from all the power rails find at least one forward biased diode path to the discharged pin. The power clamps across the power lines ensure that the voltage drop across the power lines are always clamped during the ESD stress. Thus if we look at power lines as the only CDM current sources, the internal nodes of the circuit should have a voltage level in between the two power line voltage levels and hence the chances of internal gate-oxide failure from voltage transients across the gate and source

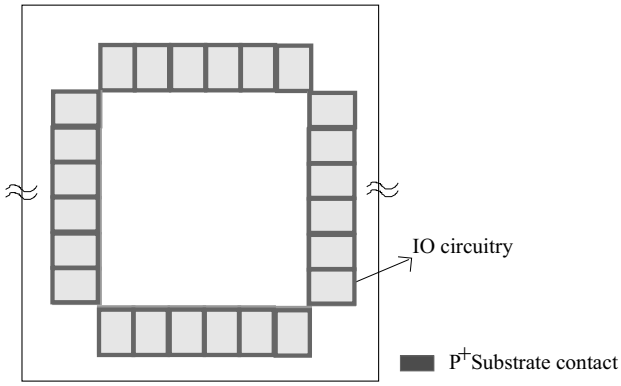


Figure 8.1: Layout of the circuit design in the IC.

nodes are small. But we have shown C_{SUB} to be the main source of CDM current and that the discharge of C_{SUB} can cause voltage transients across gate and substrate nodes as well, which can result in gate-oxide failure. Also the voltage level at the internal nodes can be affected by the parasitic contacts which the node makes with the substrate. The full chip circuit model helps us to investigate these internal voltage transients and study the cause for gate-oxide failure at these locations.

8.1.1 IC Description

The IC under study is an I/O test structure in 0.12μm technology node housed in a CDIL40 pin package. Each I/O cell also includes some basic circuitry and are interconnected to other I/O cells. In this context the core circuitry refers to the internal gate locations which are not directly connected to the I/O pins but found within an I/O cell. The overall layout of the circuit design is shown in figure 8.1.

8.1.2 CDM Measurements and Results

The IC test structures were subjected to FCDM stress and failure analysis of the failed samples showed gate-oxide failures distributed within the internal circuitry and no gate-oxide failure at the input buffers which were directly connected to the I/O pin. In this chapter, we have addressed two such failure locations found in the internal core and studied the voltage transients across

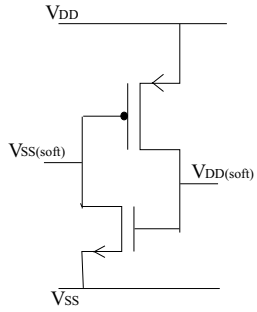


Figure 8.2: Schematic of a tie-off cell.

the gate-oxides of the MOS in this circuit during CDM stress.

1. **Tie-Off cell:** One of the CDM failure locations was a MOS of Tie-Off cells in the core circuitry. Schematic of a tie-off cell is shown in figure 8.2. It consists of an NMOS and a PMOS connected across the supply rails, such that the gate of one is connected to the drain of the other. Tie-off cell is used for providing soft grounds in the core circuitry. The failure location was at the NMOS of the tie-off cell at a CDM stress level of -500V and above. We cannot comment on which of the two MOS in the tie-off cell is more vulnerable to CDM damage as only few samples were tested.

2. **Level Shifter:** The other failure location was at the level shifter circuitry, the schematic of which is shown in figure 8.3. The failure location is at one of the first input inverters T3, whose gate is connected to the output of a core circuit at a completely different pin location.

8.1.3 Discussion

$V_{\text{gate-source}}$ at internal nodes during CDM stress

Gate-oxide breakdown is from voltage overshoot across the gate-source or gate-substrate nodes of a MOS. In the previous case study presented in chapter 7, the gate was directly connected to the discharged pad, while in this case, the gate is connected to an internal node which is in no way directly linked to the discharged pad. The gate voltage at any internal node of a circuit during CDM stress can be estimated as follows. Figure 8.4 shows the discharge current path through an internal circuit when the IC is subjected to negative CDM

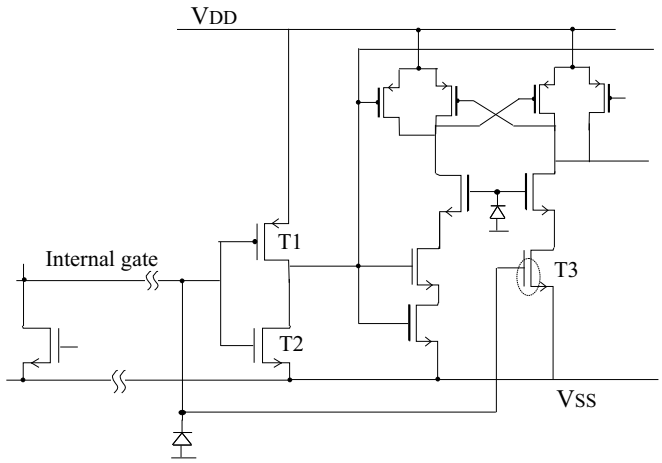


Figure 8.3: Schematic sketch of the level shifter. The failure location is marked in the circuit.

stress. Voltage drop at any internal node say, gate (or drain) node of a MOS with respect to the power lines given is given by,

$$V_{\text{gate}} - V_{\text{SS}} = V_{\text{DS}} \cdot \frac{Z_1}{Z_1 + Z_2} - [V_{\text{Z3}}] \tag{8.1}$$

where, V_{DS} is the voltage drop across the BIGFET and V_{Z3} is the potential drop along the V_{SS} bus line. Thus from equation 8.1 we see that the voltage drop across any internal node gate (or drain) and its source is always a fraction of the potential drop across the power lines. Hence the possibility of gate-oxide breakdown from voltage overshoot across gate-source nodes of a MOS with internal gate is small. But beware that locally V_{DS} can differ from the voltage drop across the power clamp depending on the amount of CDM current conducted through the V_{DD} and V_{SS} lines.

$V_{\text{gate-substrate}}$ at internal nodes during CDM stress

The substrate node is not always at the same potential as the source node of the MOS (V_{SS}/V_{DD} line). The voltage drop across the gate and substrate node of a MOS under CDM stress is given by,

$$V_{\text{gate}} - V_{\text{substrate}} = V_{\text{DS}} \cdot \frac{Z_1}{Z_1 + Z_2} - [V_{\text{R1}} + V_{\text{R2}} - V_{\text{Z3}}] \tag{8.2}$$

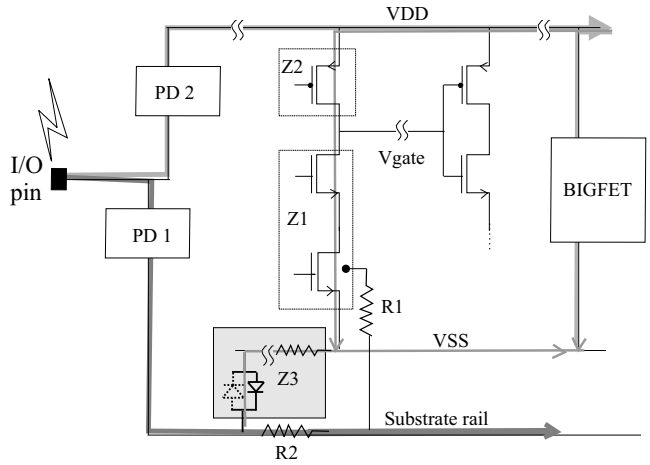


Figure 8.4: Schematic sketch of a circuit showing the discharge current path through the circuit when subjected to negative CDM stress.

where,
V_{R1} - Voltage drop between the substrate node of the MOS and the nearest P^+ substrate guard ring
V_{R2} - Voltage drop along the P^+ substrate rail between the guard ring and its contact with the V_{SS} line near the primary protection device location.
Comparing equation 8.2 and equation 8.1 we see that the excess voltage of the substrate node with respect to its source is given by,

$$V_{substrate} - V_{source} = [V_{R1} + V_{R2} - V_{Z3}] \tag{8.3}$$

To reduce this excess voltage, one should locally short the P^+ substrate contact with the V_{SS} line. In the following section, 3D full chip circuit model of the IC is built and the voltage transients across the gate-oxide of the MOS transistors in the tie-off cell and level-shifter circuit are studied. Also the influence of increasing the P^+ substrate contacts with the V_{SS} line and guard ring area on the voltage transients seen across the gate-oxide of the MOS are studied.

8.2 Building of the 3D circuit model

The full chip model is built in the following sequence, as explained in chapter 6

Step1 C_{SUB} of the IC and the dimensions of the die are determined.

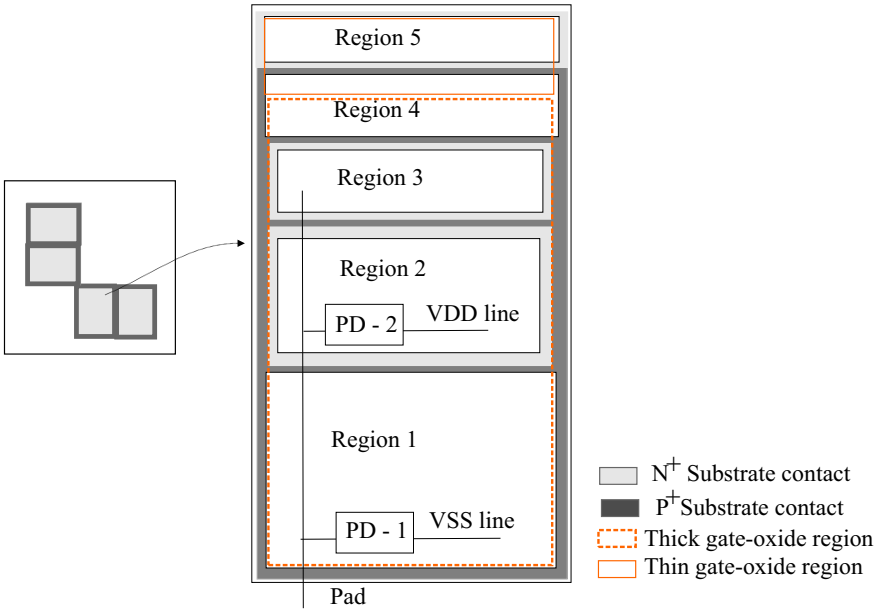


Figure 8.5: Layout of an I/O cell in the test structure showing the distribution of protection devices and circuits within each cell.

Step2 The IC design consists of a ring of I/O cells as shown in figure 8.1. Each of the I/O cell is subdivided into five regions as shown in figure 8.5. The area of each region is determined by the area enclosed by the respective guard ring around the circuit. The I/O cell region where the voltage transients are studied has the minimum grid spacing. The grid spacing else where is kept at the bond pad spacing (=80μm). Thus the substrate of the IC is modelled by 3D resistive network with suitable grid size.

Step3 The power line connection to the substrate along with their distributed bus line resistance is made. The small value of bus line sheet resistance ($\approx$ 100mΩper square) made the simulations difficult to converge. So the sheet resistance of the top power line metal layers of both V_{DD} and V_{SS} was not included. These metal layers of the power lines are treated as single nodes. The bus line contact this layer from each pin location. But other bus line resistances (interconnects in lower metal layers and via[1] are included.

[1]contact between one metal layer to another resistances

Step4 The protection device to the power lines V_{SS} and V_{DD} are present at region 1 and region 2 respectively (See figure 8.1). These protection devices are modelled by diodes in the circuit simulation. But in reality the actual protection devices between the I/O pad and the power lines in the test structure are not direct diodes, but parasitic diodes of the output drivers. The BIGFET between the V_{DD} and V_{SS} is modelled by a MOS with its gate coupled to the drain.

Step5 Next is to include the effect of other circuit elements on the voltage transients across the circuit. The actual core circuit are spread in the other regions. At these regions, the substrate is connected to the V_{DD} and V_{SS} lines through parasitic diodes. Instead of modelling the individual transistor parasitic connections to the V_{DD} and V_{SS} lines, the total area of the N^+ contacts of the source of the NMOS within the Pwell region (within that grid area) is calculated and a diode of that area is connected from the respective substrate node to the V_{SS} and likewise for V_{DD}.

Step6 The other parasitic elements of the package like L_P, C_{PIN} and the tester parasitic are measured and included in the circuit model.

Thus the entire 3D circuit model of the IC is built. Next is the study of voltage transients across the circuit when the IC is subjected to CDM stress.

8.3 Voltage transients across the Circuit

A -300V CDM stress is simulated on the circuit model of the IC test structures. The voltage drop across each substrate node with respect to the discharged pin at time $t = t_{Ipeak}$ during CDM discharge is shown in figure 8.6. The substrate voltage overshoot is maximum near the central region of the IC design where there are no circuits and minimum at locations where the protection devices are present. The actual core circuit is found in the region between the two with the CDM vulnerable, thin gate-oxide MOS closer to the central region, where the substrate voltage overshoot is much higher than the V_{hold} of the protection device. Failure analysis on these ICs show that most of the gate-oxide failure locations to be found in this weak zone confirming our reasoning. In this section, we study the voltage transients across MOS in the tie-off circuit and level-shifter when the IC is subjected to -300V CDM stress, for three different V_{SS} line contact distribution with the substrate.

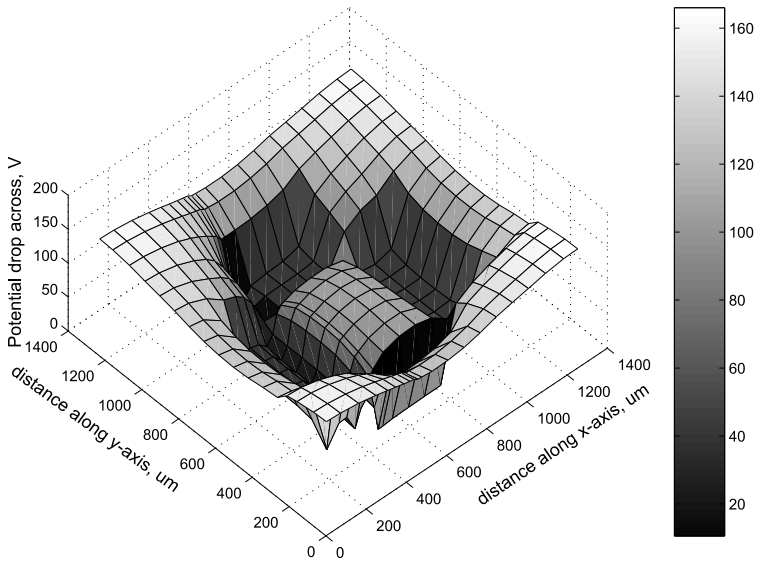


Figure 8.6: Voltage transients across each of the substrate nodes in the IC with respect to the discharged pad at 530ps during -300V CDM stress.

One contact: Connections are given as in the circuit design. The V_{SS} line contacts the substrate at the discharge pin location. Also V_{SS} line is connected to the V_{DD} through BIGFET power clamp.

Contact at each I/O pin location: V_{SS} line is well shorted to the substrate rail at each pin location. This increases the effectiveness of the guard ring in reducing the substrate potential.

Smaller guard ring area: Placement of additional guard ring within the guard ring present around the MOS to be protected. This decreases the amount C_{SUB} discharge current flowing through the substrate.

8.4 Level Shifter Circuit

The equivalent circuit of the level shifter circuit used in the simulation as shown in figure 8.7. An internal node (input to an output buffer) is connected to the gate of T1, T2 and T3 MOS transistors at a completely different location. The failure location was found to be at the gate-oxide of T3. But as the number

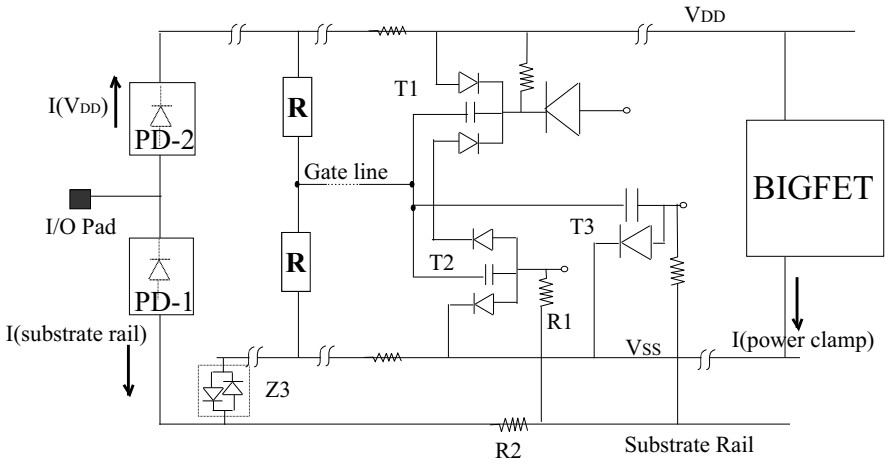


Figure 8.7: Equivalent circuit of the level shifter circuit used in the simulation to study the gate-oxide voltage transients.

of samples tested were few, we did not know which of the three is most vulnerable to CDM damage. This circuit is especially very interesting for our study as all the three transistors are present at different locations in the layout. The layout of these transistors and the P^+ substrate contact distribution is shown in figure 8.15. As the absolute value of the gate capacitors of T1, T2 and T3 is too small (in the order of few femto farad), their influence on the voltage level of the gate line is also small and hence is neglected in our analysis. Instead we assume that the voltage level of the gate line is only determined by the voltage levels of the power lines at the location where it connects to it through MOS. During negative CDM stress, the discharge current from C_{SUB} sees two possible paths to the grounded pin as shown in figure 8.8. One, through the forward biased diode clamp of V_{DD} and the BIGFET, and the second through the reverse biased diode clamp to the substrate rail. A rail based protection is designed to conduct through the former.

8.4.1 One contact

In this case, the circuit connections are as given in the actual test structure. Figure 8.9 shows the relative amount of discharge current flowing through the substrate rails, V_{DD} and the BIGFET power clamp during the negative CDM stress. From the figure we see that in the initial time of discharge, majority of the current is conducted through the diode to the V_{DD} line. But soon after-

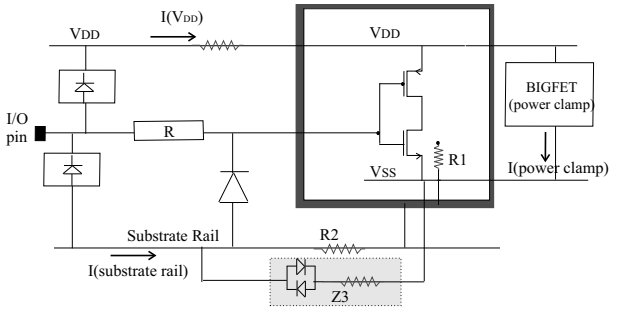


Figure 8.8: Discharge current path through the circuit.

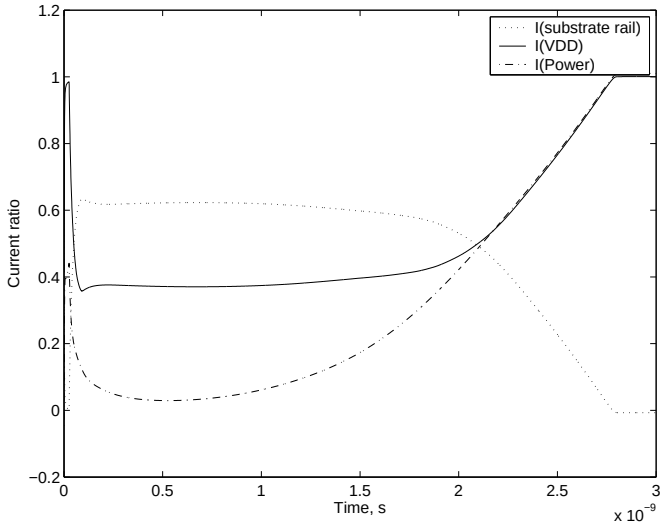


Figure 8.9: Relative amount of current conducted through the V_{DD}, substrate rail and the BIGFET during -300V CDM stress.

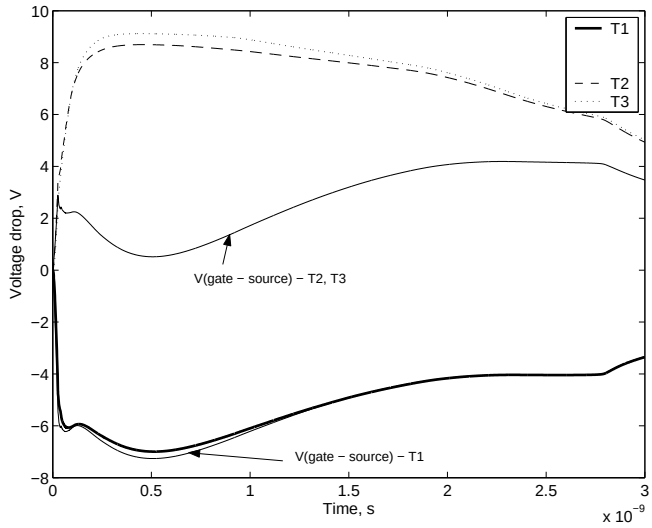


Figure 8.10: Voltage transients across the gate-oxide of MOS T1, T2 and T3 in the level shift circuit, when the IC is subjected to CDM stress in Case A. Thin lines correspond to $V_{\text{gate-source}}$.

wards, most of the discharge current is conducted via the substrate rail clamp. This can be explained as follows. The V_{SS} line has only one short contact to the substrate rail. Hence the amount of current conducted through the V_{SS} line into V_{DD} (through BIGFET) is very much limited. When the potential drop across the substrate rail clamp reaches the clamp turn-on voltage, most of the discharge current will be directed through this clamp. As a result the potential drop across the substrate rail will be high and hence the effectiveness of the guard ring will be reduced. This is reflected in the large voltage drop across the gate-substrate nodes of T2 and T3 as compared to its gate and source nodes as shown in the figure 8.10. The potential drop across the gate and substrate nodes of T3 is slightly higher than that of T2. This increase in potential drop across T3 is attributed to the larger area of the guard ring in which T3 is present. Also note that the voltage drop across the gate and source node of T1 (gate and V_{DD} line) is greater than that of T2 or T3 (gate and V_{SS}). This cannot happen if our argument that the power internal node is the average value of the power lines is correct. One should remember that the gate line connected to T1, T2 and T3 comes from a completely different location. Depending on the different amount of current conducted through the two power lines, the local potential drop across the two power lines can vary significantly because of the

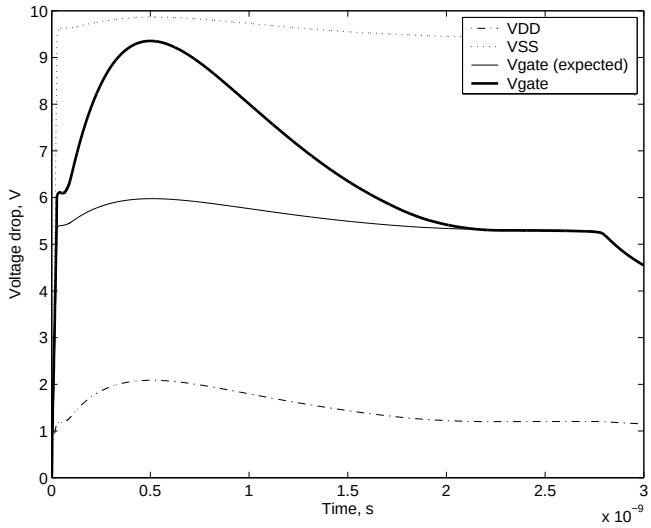


Figure 8.11: Voltage transients in the gate, V_{SS} and V_{DD} lines during -300V CDM stress.

bus line resistance. Figure 8.11 shows the voltage transients at the gate line and the two power lines V_{DD}, V_{SS} at the location of the level shifter circuit, with respect to the discharge pad. Also shown in the figure is the estimated gate line voltage level at the location of the level shifter circuit. From the figure we see a significant difference between the expected and actual gate potential. With regard to T1, the voltage transients across the gate and substrate nodes do not vary very much from it voltage transients across its gate to source voltage (See figure 8.10). In other words, the source and substrate nodes of T1 are at the same potential level. This is because the N^+ substrate contact of the Nwell is shorted to the V_{DD} line and the amount of CDM current conducted through Nwell is too less to be seen.

8.4.2 Contact at each I/O pin location

The effect of shorting V_{SS} to the substrate rails at each pin location is studied in this section. By increasing the number of V_{SS} line contacts, the current conducted from the discharged pin to the V_{SS} is increased. This is shown by the increase in the amount of current conducted through the BIGFET power clamp in figure 8.12. The relative amount of current conducted through the V_{DD}, substrate rail and the BIGFET is shown in the figure. Nevertheless, there

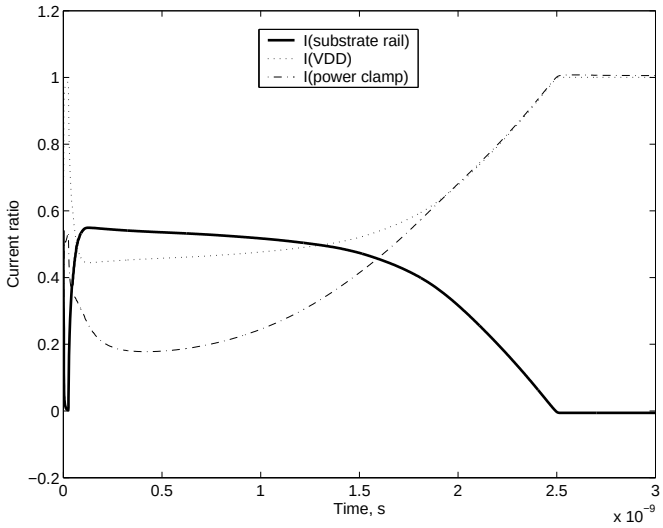


Figure 8.12: Relative amount of current conducted through the V_{DD}, substrate rail and the BIGFET during -300V CDM stress with increased substrate line contacts to the V_{SS}.

is considerable amount of current being discharged directly through the reverse biased diode (of output driver) clamp to the substrate rail. The voltage drop seen across the gate-oxides of T1, T2 and T3 when the IC is subjected to $-300V$ CDM stress is shown in figure 8.13. From the figure, we see that with increased substrate contacts, the voltage transients across the gate and substrate nodes of both T2 and T3 are reduced drastically, even below its voltage drop across the gate and source nodes. Note that the voltage drop across the gate and substrate nodes of T3 is higher than that of T2. This difference is in accordance with our reasoning that the larger the guard ring area is, the larger is the potential drop. The voltage transients seen by the gate and the two power lines V_{DD} and V_{SS} at the location of the level shifter circuit, with respect to the discharge pad in this case is shown in figure 8.14. The voltage at the gate is closer to the voltage of the V_{SS} at the location of the level shifter. As a result, the voltage transients across the gate and V_{DD} line (source of T1) is found to be higher than the voltage transients across the gate and V_{SS} line (source of T2 and T3). This need not be the case always. If the gate line happened to be closer to the power clamp, then the gate line voltage might be closer to V_{DD} line potential. As mentioned earlier in section 8.5.2, the danger of local voltage drop across the power lines going much higher than the clamping voltage

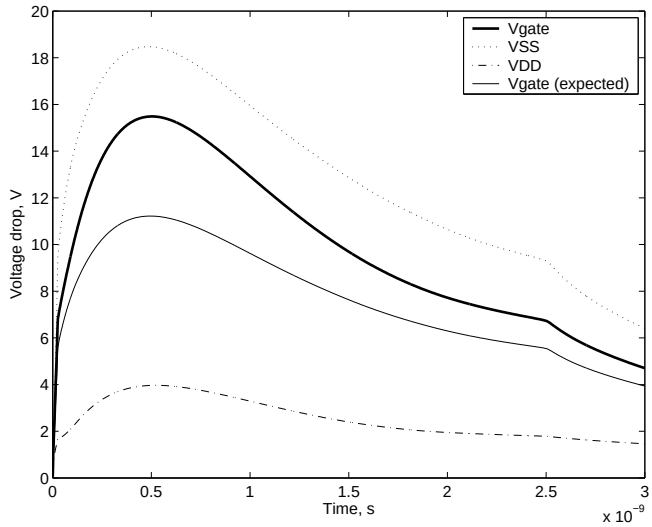


Figure 8.13: Voltage transients across the gate-oxide of MOS T1, T2 and T3 in the level shift circuit, when the IC is subjected to CDM stress in Case B.

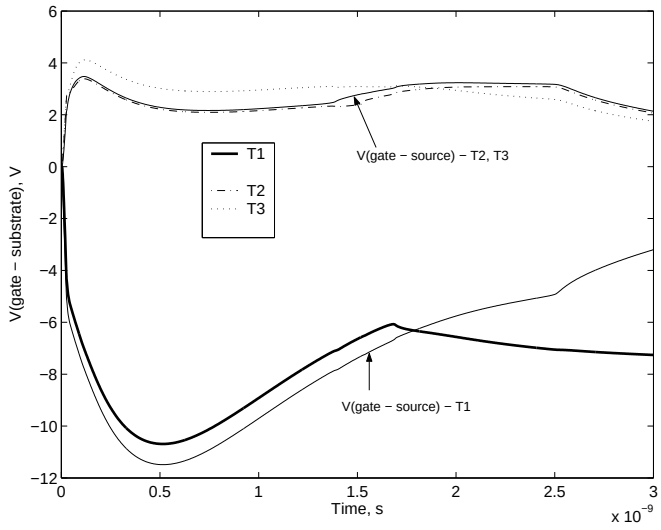


Figure 8.14: Voltage transients in the gate, V_{SS} and V_{DD} lines during -300V CDM stress when the V_{SS} line is well shorted to the substrate rail.

of the power clamp, can be reduced by providing distributed clamps across the two power lines. This will also ease in the equal distribution of CDM current through both the power lines. The voltage transients across the gate-oxide of the T1 in the level shifter circuit is similar to the voltage transients across the PMOS in the tie-off cell studied in section 8.5. The substrate below the Nwell of T1 discharges through the substrate into the V_{SS} line rather than flowing through the Nwell into the V_{DD} line and thereby causing the voltage transient across the gate and source nodes to be higher than the gate-substrate nodes of the PMOS.

8.4.3 Smaller guard ring area

In this section, we study the effect of reducing area enclosed by the guard ring on the voltage transients seen across the MOS inside it. Figure 8.15 shows the original and modified distribution of the substrate contacts respectively. Figure 8.16 shows the voltage transients across the gate-oxides of the MOS T1, T2 and T3 in the level shifter circuit when the IC is subjected to -300V CDM stress. By reducing the spacing between the substrate node and its P^+ substrate contact, we expect to reduce the voltage difference between the substrate and source nodes, assuming the source nodes are shorted to the P^+ substrate contact. Our expectation is affirmed by the slight reduction in the voltage transients seen across the gate and substrate nodes of T3. The presence of smaller guard ring area around T1 does not affect its gate-oxide voltage transients, as the discharge path of the substrate below Nwell is not through the Nwell but through the p-substrate into P^+ substrate contact.

8.5 Tie-Off Cell

The equivalent circuit of a tie-off cell used in the simulation is as shown in figure 8.17. The $V_{SS(soft)}$and $V_{DD(soft)}$lines are connected to the V_{SS} and V_{DD} lines through one or more MOS transistors. As we study the CDM stress behavior of the IC when it is not powered up, the conduction through these devices is minimum. To keep the simulations simple, we replace these MOS by large resistors R. As both the $V_{SS(soft)}$and $V_{DD(soft)}$lines are treated as floating nodes, inclusion of R (=5000Ω) helps the simulator determining the voltage at these internal nodes. The inclusion of R sets

$$V_{SS(soft)} = V_{DD(soft)} = \frac{1}{2}V_{DS}$$

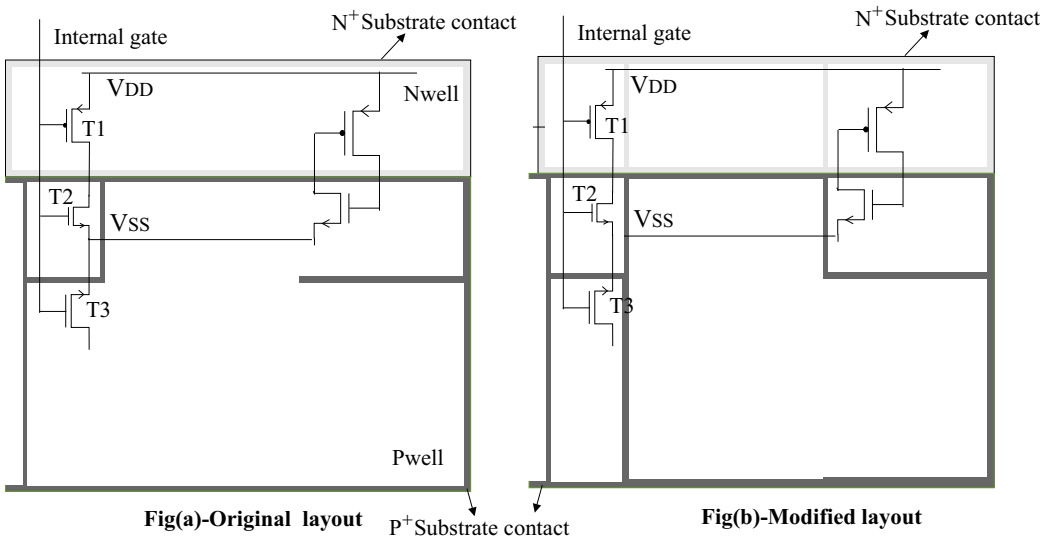


Figure 8.15: Layout of the transistors along with the P^+ substrate contact distribution.

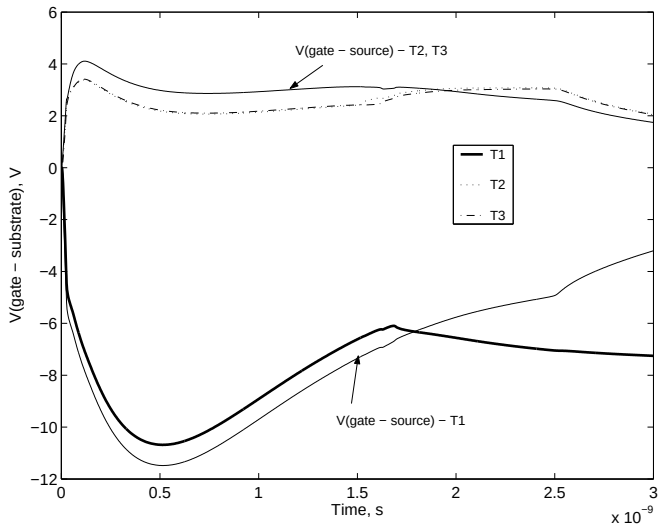


Figure 8.16: Voltage transients across the gate-oxide of MOS T1, T2 and T3 in the level shift circuit, when the IC is subjected to CDM stress in Case C. Thin lines correspond to $V_{\text{gate-source}}$.

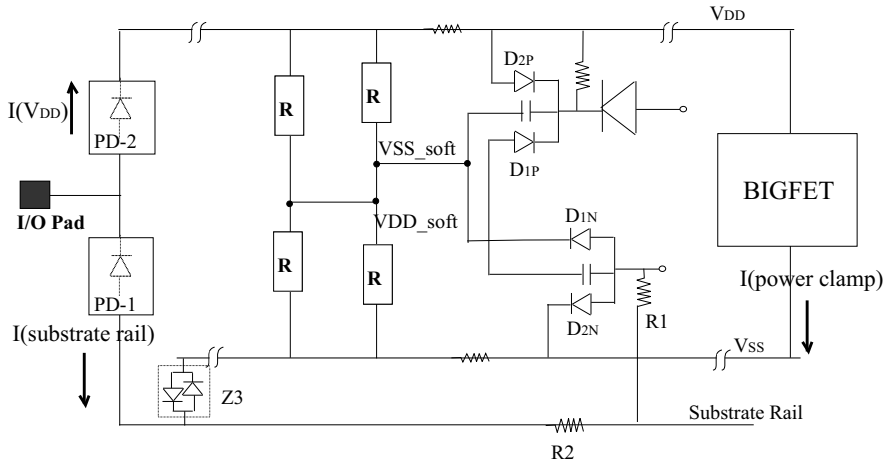


Figure 8.17: Equivalent circuit of the tie-off cell used in the simulation to study the gate-oxide voltage transients.

8.5.1 One contact

The voltage transients across the gate-oxides of the NMOS and PMOS of the tie-off cell, when the IC is subjected to -300V CDM stress is shown in figure 8.18. During negative CDM stress, the output driver to the V_{DD} is forward biased and that of the V_{SS} is reverse biased. The voltage at any node between these two should be an average of the voltage levels at the two power lines. But these internal nodes also have parasitic connection to the substrate. The extent to which the internal voltage level varies from its average value depends on its parasitic connection to the substrate.

Voltage transients across NMOS

Consider the internal node $V_{\mathrm{DD(Soft)}}$. This node is connected to the Nwell of the PMOS through diode $D_{1\mathrm{P}}$ and to the substrate of NMOS through its gate capacitor $C_{\mathrm{gate(N)}}$. During negative CDM stress, $D_{1\mathrm{P}}$ is reverse biased. Hence $D_{1\mathrm{P}}$ will have influence only if the voltage across it exceeds its junction breakdown voltage. The voltage at the substrate node of the PMOS is strongly coupled to the V_{DD} line potential because of the forward biased diode $D_{2\mathrm{P}}$. The

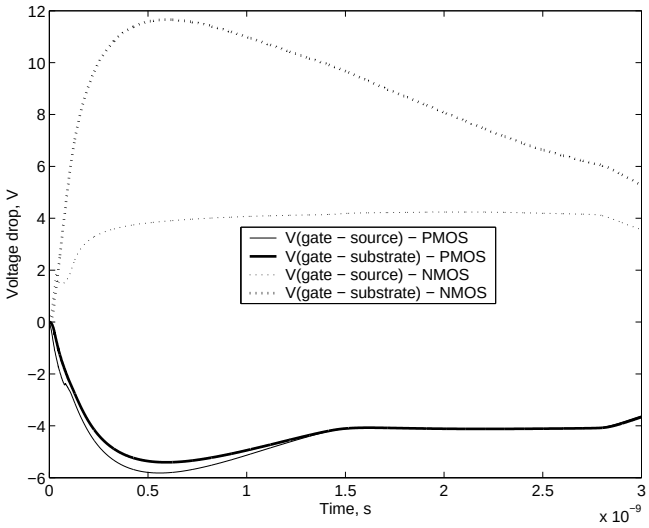


Figure 8.18: Voltage transients across the gate-oxide of MOS in the tie-off cell when the IC is subjected to CDM stress in Case A.

influence of $C_{\text{gate(N)}}$ on the voltage level at $V_{\text{DD(soft)}}$ depends on its magnitude and the rate of change of voltage across it. But as the magnitude of $C_{\text{gate\_N}}$ is in the order of only few femto farad, its influence on the voltage level of internal node is limited to the initial transients of the CDM stress. Thus the voltage level of the internal node $V_{\text{DD(soft)}}$ is almost at the average value of the voltage levels at V_{DD} and V_{SS} lines at the location of the tie-off cell circuit, for most of the time during the CDM discharge. Figure 8.18 shows that the voltage transients across the gate-source nodes is much lower than the voltage transient across its gate-substrate node. This is because the amount CDM current conducted through V_{SS} line is much lesser than the current conducted by P^+ substrate rail resulting in

$$V_{\text{R1}} + V_{\text{R2}} \gg V_{\text{Z3}}$$

Voltage transients across PMOS

Let us now consider the other internal node $V_{\text{SS(Soft)}}$. Similar to $V_{\text{DD(Soft)}}$, $V_{\text{SS(Soft)}}$ is also almost at the average value of the local bus line potentials. This node is connected to the substrate of NMOS through $D_{1\text{N}}$ and to the substrate of PMOS through its gate capacitor $C_{\text{gate(P)}}$. Note that though $C_{\text{gate(P)}}$ is larger

than $C_{\text{gate(N)}}$ by a factor of three, its influence on the voltage level of $V_{\text{SS(soft)}}$ would be very less as the potential drop across it is less. (substrate node of PMOS being well connected to the V_{DD}). From figure 8.18 we see that unlike the gate-substrate voltage of NMOS, the voltage drop across the gate-substrate nodes of the PMOS does not vary from its voltage drop across its gate and source nodes. This is because the N^+ substrate contact of the Nwell region is directly connected to the V_{DD} line. The maximum voltage across the substrate node of the PMOS and the V_{DD} line potential can be $\approx$ 1V (forward biased diode $D_{2\text{P}}$. The fact that the substrate and source seem to be at the same potential indicates that the amount of CDM current discharging through the Nwell is too less to be seen.

8.5.2 Contact at each I/O pin location

In this case, the V_{SS} line is locally shorted to the substrate rails at all the pin locations. By locally shorting the V_{SS} line contacts to nearby, we aim at making,

$$V_{\text{Z3}} - V_{\text{R2}} \approx 0$$

in equation 8.4. As a result the voltage difference between the source and substrate nodes will only depend on the amount of discharge current flowing from its substrate node to the P^+ substrate contact $i.e.$ V_{R1}. By increasing the number of V_{SS} line contacts with the substrate rail, the current conducted through the V_{SS} line and hence through the BIGFET is increased (See figure 8.12). The voltage transients across the gate-oxide of the MOS in the tie-off during $-300V$ CDM stress on the circuit with well distributed V_{SS} line contacts with the substrate rail is shown in figure 8.19.

Voltage transients across NMOS

From figure 8.19, we see that the voltage transients across gate-substrate nodes of the NMOS has been drastically reduced as compared to its transients when there was only one substrate rail contact. In fact the voltage drop across the gate and substrate nodes of the NMOS goes even below its voltage transients across its gate and source nodes. This is because, by increasing the current conducted through the V_{SS} line,

$$V_{\text{Z3}} \gg [V_{\text{R2}} + V_{\text{R1}}]$$

Plugging this state in equation 8.4, we get

$$V_{\text{substrate}} - V_{\text{source}} = V_{\text{R1}} + [V_{\text{R2}} - V_{\text{Z3}}] < 0$$

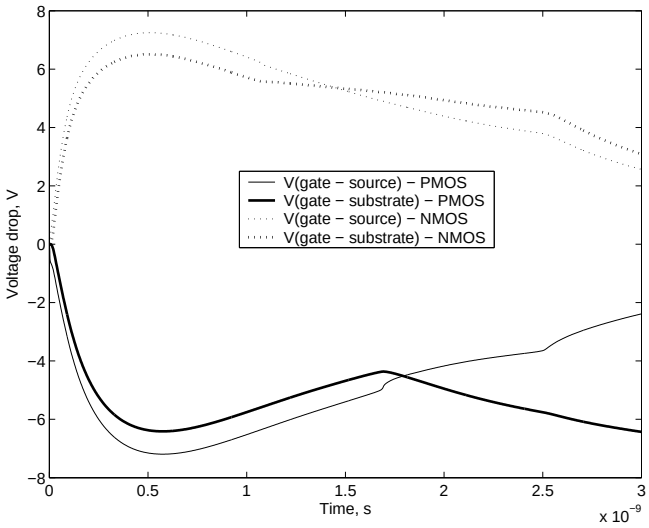


Figure 8.19: Voltage transients across the gate-oxide of MOS in the tie-off cell when the IC is subjected to CDM stress in Case B distribution.

Note that the potential drop across the gate and source nodes has been increased as compared to the previous case which had one substrate contact. The increase in the voltage drop across the gate and source nodes arises from the increased amount of CDM current conducted through the two power lines and the accompanying voltage drop along these lines.

Voltage transients across PMOS

Figure 8.19, shows that the voltage transients across the gate-source nodes of the PMOS is higher than it gate-substrate nodes. This can be explained as follows. The Nwell of the PMOS is connected to the common p-substrate on which the Pwell is also present. By shorting the V_{SS} line to the P^+ substrate contact, the substrate below Nwell discharges through the p-substrate into the V_{SS} line instead of flowing into the V_{DD} through the Nwell. Thus the potential of the substrate node of PMOS is pulled closer to the V_{SS} line. But as the diode D_{2P} is forward biased, the maximum potential drop between the substrate and source nodes of the PMOS is limited to the knee voltage of the diode D_{2P} which is $\approx$ 1V.

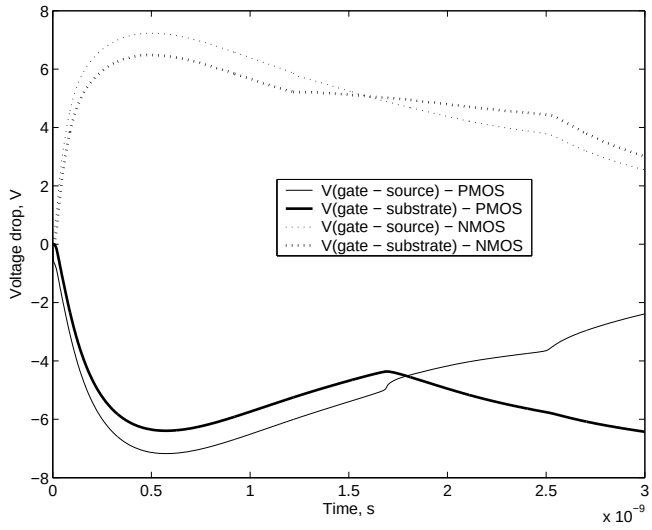


Figure 8.20: Voltage transients across the gate-oxide of MOS in the tie-off cell when the IC is subjected to CDM stress in Case C.

8.5.3 Smaller guard ring area

In this section, we study the effect of the area of the guard ring on the voltage transients seen across the MOS. Figure 8.15 shows the original and modified distribution of the substrate contacts respectively. The V_{SS} lines being shorted to the substrate rails at each pin location, the voltage drop across the substrate node and the corresponding guard ring is determined by the area of the guard ring and the amount CDM current discharged through it.

Voltage transients across NMOS

Figure 8.20 shows the voltage transients across the gate-oxide of the MOS in the tie-off cell when placed in a smaller guard ring area. From the figure, we that reduction area enclosed by guard ring shows only a very slight reduction in the voltage drop across the gate and substrate node. The effect of the substrate contact distribution would have been more effective had the bus line resistance been totally neglected.

Voltage transients across PMOS

Figure 8.20 shows that the reduction in the area of the N^+ guard rings does not cause any notable change in the voltage transients across the gate-oxide of the PMOS of the tie-off cell with the reduced area enclosed by the guard ring. This is because all the discharge current from the substrate in the Nwell region is flowing through the p-substrate into the V_{SS} line rather than discharging through the Nwell into the V_{DD} line.

8.6 Conclusions

The 3D full chip circuit model helps us to analyse both the voltage transients across both gate-source and gate-substrate nodes of MOS during CDM stress. It also helps to investigate the influence of parasitic substrate contacts on the voltage level at the internal nodes of a circuit. From the analysis we find that the internal gate-oxide failure at the tie-off cell and level-shifter circuit is mainly from the voltage transients across the gate and substrate nodes of the MOS. In the tie-off cell, the MOS subjected to maximum voltage transients is the NMOS and at the level-shifter it is the NMOS T3. Local shorting of the V_{SS} line to the P^+ substrate contact at each pin location greatly reduces the danger of gate-oxide failure. Placement of CDM sensitive (thin gate-oxide) MOS within a small guard ring area whose substrate contact is well shorted to the power rails would greatly help in reducing the difference between the substrate and source voltages of the MOS. The effect of reducing the area enclosed by the guard ring did not make any notable reduction in the voltage drop across the gate and the substrate node. This is because of the significant amount of voltage drop along the bus lines. The effect of substrate contact distribution can be more effectively studied if the bus line resistances had been totally neglected.

The bus line resistances should be taken into account if the current conducted through these lines are significant. As a result of bus line resistance, the presence of a power clamp across the two power lines V_{DD} and V_{SS} will not be effective in clamping the voltage drop them locally. The difference in the amount of CDM current conducted along these lines add up to the effect. Distribution of power clamps between the two power lines V_{DD} and V_{SS} will help to ensure proper clamping of the voltage drop across them by distributing the CDM current through both the power lines.

Conclusions

In this chapter the main conclusions of the CDM aspects of different individual elements of an IC studied in this thesis are summarized. In addition conclusions on the application of this work are given in the form of general design guidelines.

CDM discharge currents reach very large amplitudes of current (few ampere) in a fraction of a nanosecond. This places an additional requirement on the protection devices to have a turn-on time shorter than the rise time of the CDM pulse. CDM measurements on protection devices (ggNMOSt and LVTSCRt), show that devices with gate-length shorter than 0.5μm comply to this requirement and are therefore suitable as CDM protection devices [chapter3]. The IO buffers being at the interface between the external world and the internal circuitry are one of the weakest locations to CDM failure. Simulation shows that only in the presence of additional protection devices, the decoupling resistor helps in reducing the voltage across the IO buffers [chapter4].

CDM performance of an IC is highly influenced by its package type. This makes practical evaluation of CDM robustness of a given circuit design independent of its package impossible. However it has been shown that there is a suitable method by which the CDM failure level of a circuit in one package type can be extrapolated to its CDM performance in other packages based on our simulation model. The main hinderance towards developing a suitable protection circuit against CDM stress is the lack of knowledge on the source of CDM discharge current and its discharge path through the IC. The various capacitors formed between the conducting layers of the IC and the package are identified as the CDM current sources. The capacitance formed by the die attachment plate with the package, C_{SUB} is found to be the largest. Moreover

the discharge of C_{SUB} poses an additional threat of CDM failure from voltage overshoot between the substrate and the circuit elements. Hence its inclusion into the circuit model used to evaluate the CDM performance of a circuit is mandatory.

A 3D circuit model which includes C_{SUB} and its discharge path through the substrate into the grounded pin is proposed. From the simulations, we see a large voltage drop between the substrate and the circuit elements during CDM stress. This voltage drop at a particular location depends on its distance to the closest substrate contact and its substrate resistivity. Simulation shows that for the currently available protection designs (both pad based and rail based) to be effective in clamping the gate voltage below its breakdown threshold, the number of substrate contacts to the supply lines has to be increased such that the potential at the substrate nodes are closer to its source nodes [chapter 7 and chapter 8]. Therefore, in addition to the currently available design guidelines, increase of substrate contact to power lines should be included for CDM protection.

Although the proposed model needs fine tuning (net-list reduction and simulation stability) before it can be directly used by the IC design engineers to evaluate the CDM performance of an IC, a fairly good estimate of the regions viable to CDM damage from voltage overshoot between the substrate and the circuit elements can be identified by including the P^+ substrate contacts to the substrate rail and the V_{SS} and V_{DD} line contacts with the substrate rail alone. Note that to this end only a fraction of the total design is needed (substrate contact with the supply lines).

General design recommendations to ensure CDM protection
From our study on the various designs that affect the CDM performance of an IC, we recommend the following:

- Ensure turn-on time of the protection devices to be shorter than the rise time of the CDM pulse [chapter 3].

- Provide distributed substrate line contacts with the V_{SS} and V_{DD} power lines such that CDM discharge current flows through the power lines (low resistance) and not through the substrate (high resistance) [chapter 7] and [chapter 8].

- Metal line interconnects of the V_{SS} and V_{DD} power lines to the protection devices are narrow metal lines which have high effective resistance.

Ensure the resistance of these metal line interconnects to the protection devices to be small.

- To avoid discharge current flow through the internal circuit, the voltage drop across the power lines should be maintained below the minimum threshold value required to turn-on the internal MOSts. For this, the clamping device across the power lines should also be distributed.
- CDM sensitive (thin gate-oxide) MOSts should be placed within small guard ring areas whose substrate contacts are shorted to the respective power lines in that circuitry.

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